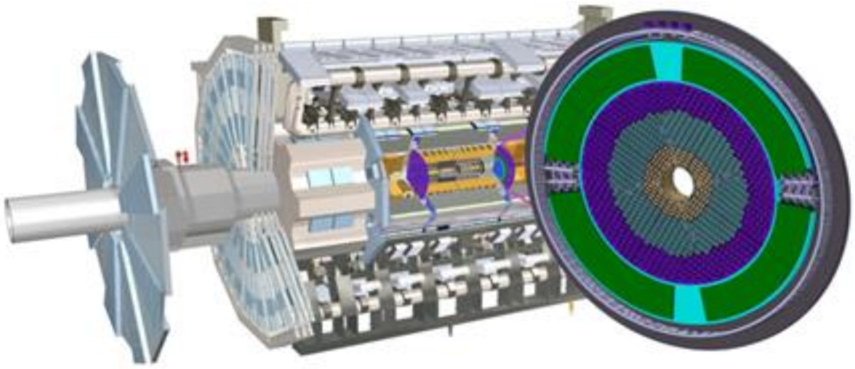
Ongoing validation of the High Granularity Timing Detector (HGTD) demonstrator for the ATLAS phase II upgrades



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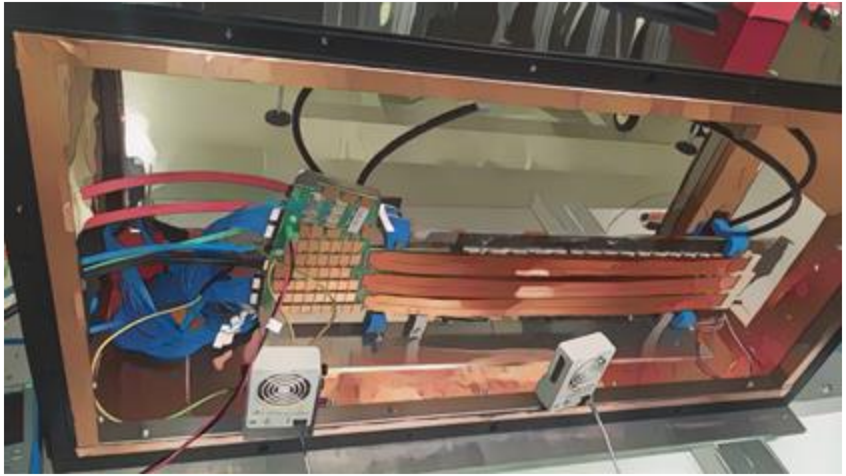
in collaboration with ATLAS HGTD GROUP
8th July 2025

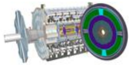
University of the Witwatersrand

Outline

- ❑ Introduction ATLAS HGTD
- ❑ Motivation
- ❑ ATLAS HGTD Demonstrator
- ❑ Validation and tests results
- ❑ Test beam Activities
- ❑ Summary and outlook



First, why is the HGTD needed?

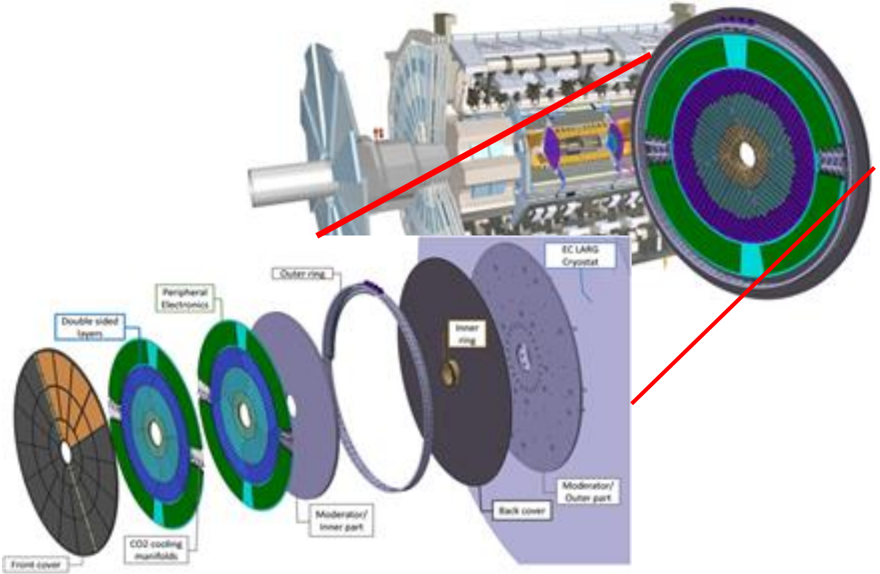


Introduction to ATLAS HGTD

- **Upgrade Timeline:** ATLAS will install the high granularity timing detector (HGTD) in the endcap region during the Phase-II upgrade (2026) to cope with HL-LHC conditions.

- **Primary Goal:** Improve pile-up mitigation by adding precision timing information (target resolution: 30–50 ps/track).

- **Sensor Technology:**
  - LGADs (Low-Gain Avalanche Detectors) for high precision timing
  - Pixel size: 1.3 × 1.3 mm²
- **Geometry:**
  - Pseudorapidity: $2.4 < |\eta| < 4.0$
  - Radial range: 12 cm < R < 64 cm
  - z-position: ~3.5 m, total thickness: 7.5 cm
  - 2 double-sided layers per endcap

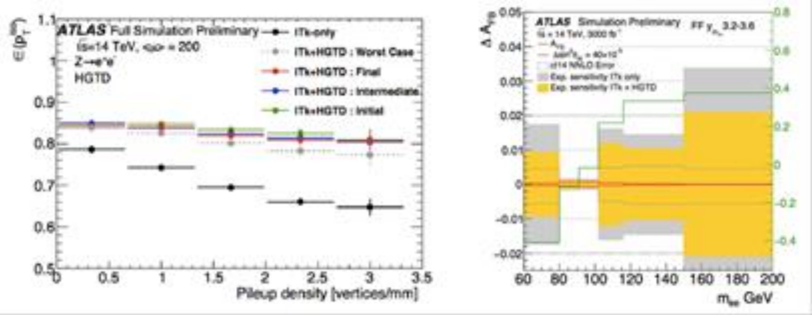


- **Performance Targets:**
  - Occupancy < 10%
  - Radiation hardness: up to 3.7×10^{15} neq/cm², 4.1 MGy
  - Average hits/track: 2–3, depending on R

Physics Motivation

Pileup Challenge at HL-LHC

- Multiple collisions occur close in space but separated in time → pileup background
- 30 ps timing resolution needed to reduce pileup by a factor of 6



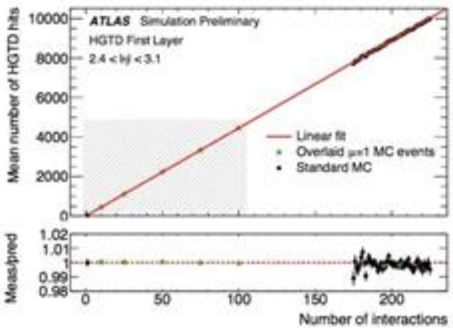
ATL-PHYS-PUB-2018-037.pdf

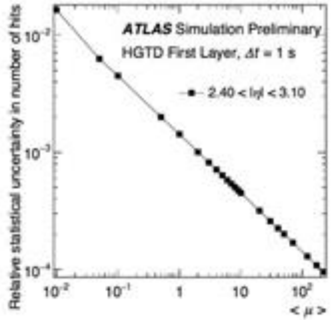
HGTD Impact

- Enhances forward electron ID by separating electrons from pileup jets with precise timing (~30 ps)
- Improves weak mixing angle measurements in high pileup
- Sensitivity gains in Drell–Yan channels:
  +13% in Central–Forward (CF)
  +25% in Forward–Forward (FF)
- Increases electron purity → better electroweak precision

Luminosity Measurement

- 1% precision required at HL-LHC for Higgs physics
- HGTD's high granularity → low occupancy & linear hit rate
- Enables bunch-by-bunch luminosity estimation via fast readout





https://cds.cern.ch/record/2623663/files/LHCC-P-012.pdf

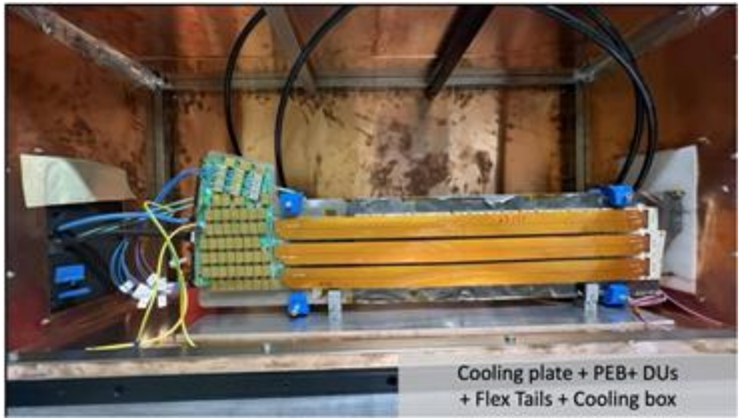
HGTD Demonstrator Overview

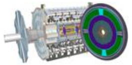
Purpose

- To validate the design, performance, and integration of the High Granularity Timing Detector (HGTD) components for the ATLAS Phase-II Upgrade.

Goals of the Demonstrator

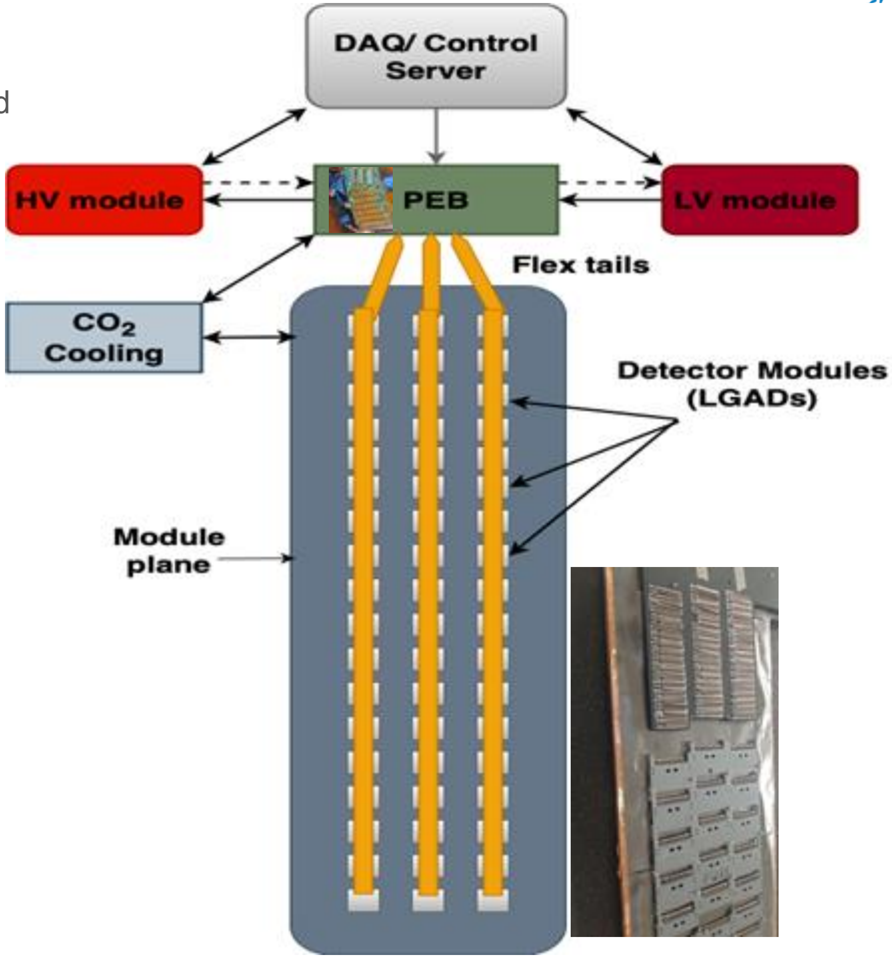
- Evaluate sensor timing resolution (~30 ps)
- Test radiation hardness and thermal performance
- Validate mechanical and electrical integration
- Provide input for final HGTD system design





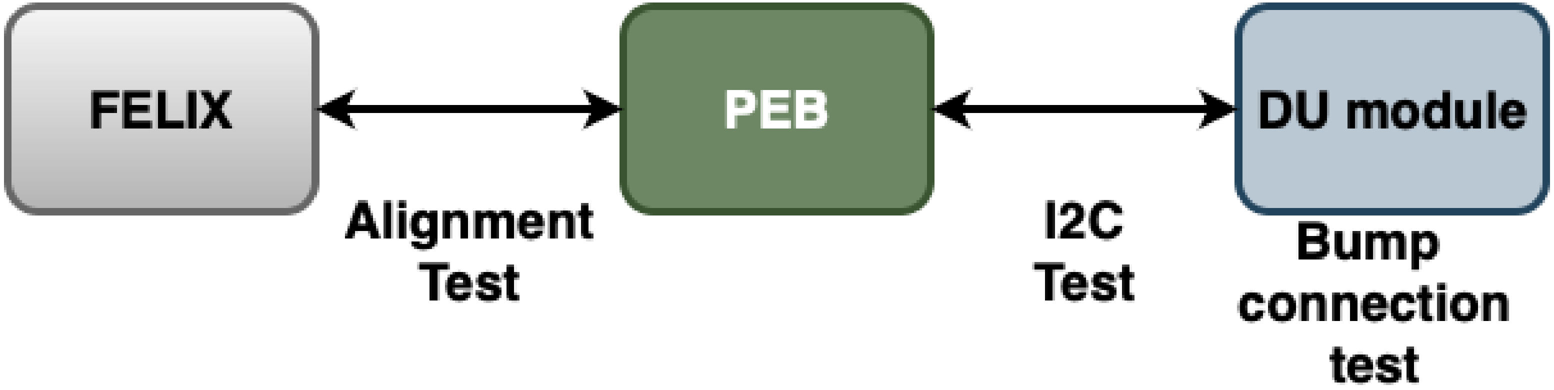
Demonstrator setup

- High voltage (HV) to deplete the LGAD sensor and create a strong electric field inside it.
- Low Voltage (LV) to power the front-end electronics that read out and process signals from the LGADs.
- Peripheral electronic board (PEB) distributes power (HV and LV), monitors environmental conditions (like temperature and humidity), and interfaces with the DAQ system to ensure safe and stable operation of the HGTD modules.
- LGAD Modules ×54 (assembled with readout ASICs)
- Flex Tails for signal and power routing
- CO_2 Cooling System to maintain thermal stability under realistic power loads
- DAQ Server for synchronized data acquisition and control



Validation tests

- Connected all the flex tails with the PEB and 54 Modules
- Alignment test (Ensures all components are correctly positioned and functioning.)
- I2C Test: Checks communication with the module by writing to a register and reading it back.
- Scanning test (To check bump connections)
- Power test (To validate the power consumption of modules)



Alignment test

Purpose: Ensure all lpGBT (Low-Power Gigabit Transceiver) links are correctly aligned before data acquisition (DAQ)

Initial step: Run `python3 peb_prep.py -G x`

→ Disables equalization, enables pre-emphasis

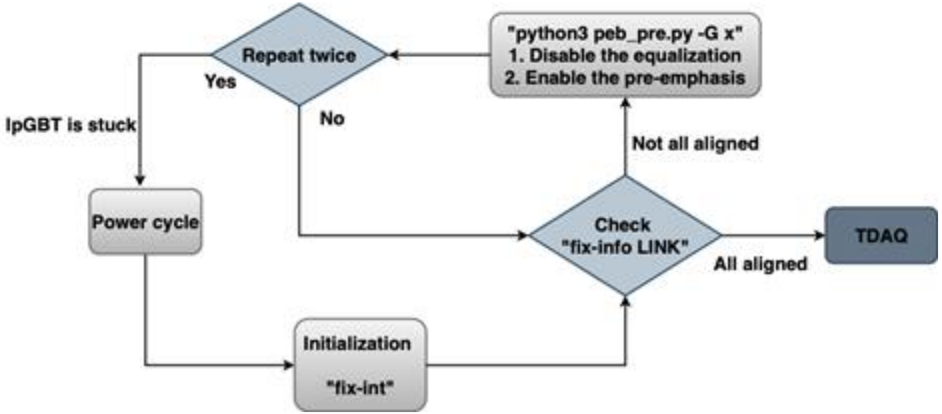
Use `flx-info LINK` to check alignment status:

- If not aligned → repeat alignment up to 2 times
- If still stuck → power cycle and re-initialize with `fix-init`

Once all links are aligned → proceed to DAQ

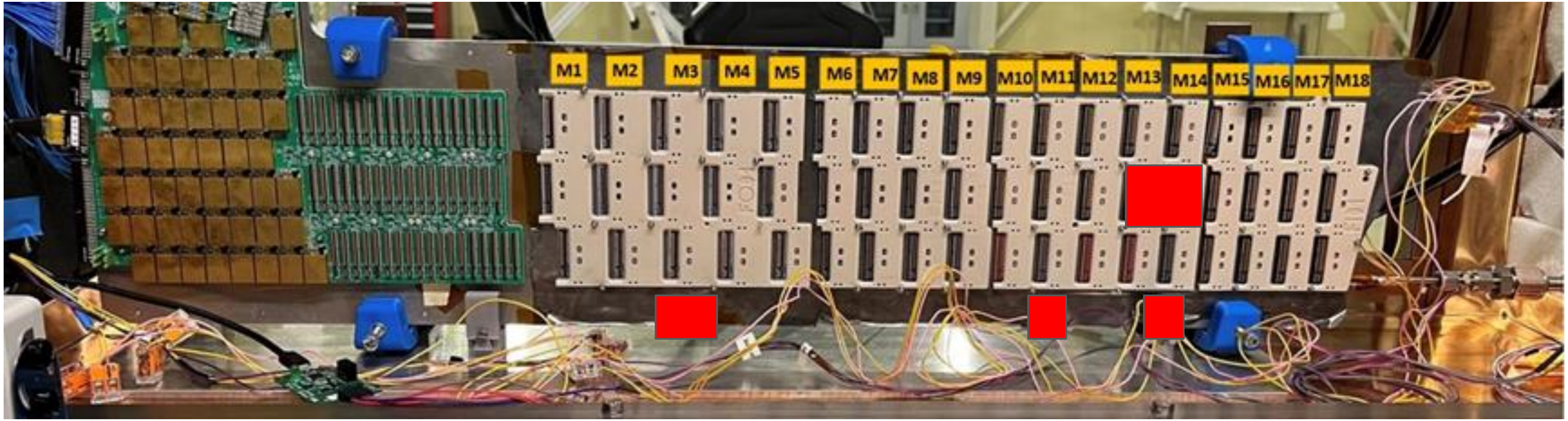
```
Link alignment status
------------------------
Channel | 0    1    2    3    4    5    6    7    8    9
          -------------------------------------------------
Aligned | YES  YES  YES  YES  YES  YES  YES  YES  YES  NO

Channel | 10   11   12   13   14   15   16   17   18   19
          -------------------------------------------------
Aligned | NO   NO   YES  NO   YES  NO   NO   NO   NO   NO
```



From the I2C tests

- ❑ Some modules didn't pass the I2C tests. Shown with the



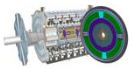
Threshold Scans with HV ON/OFF – Purpose & Method

Purpose

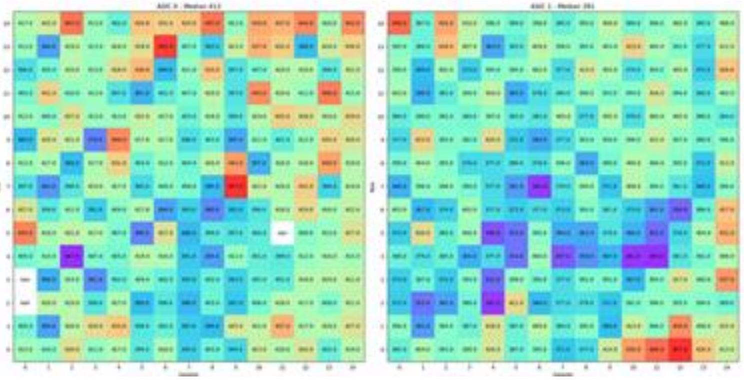
- To verify bump bonding and charge collection efficiency of the sensor.
- To observe how the presence of electric field (HV ON) affects the detector's response compared to HV OFF.

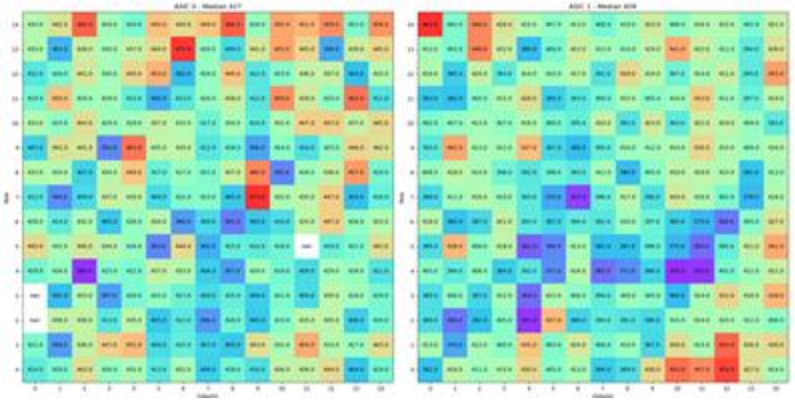
Procedure

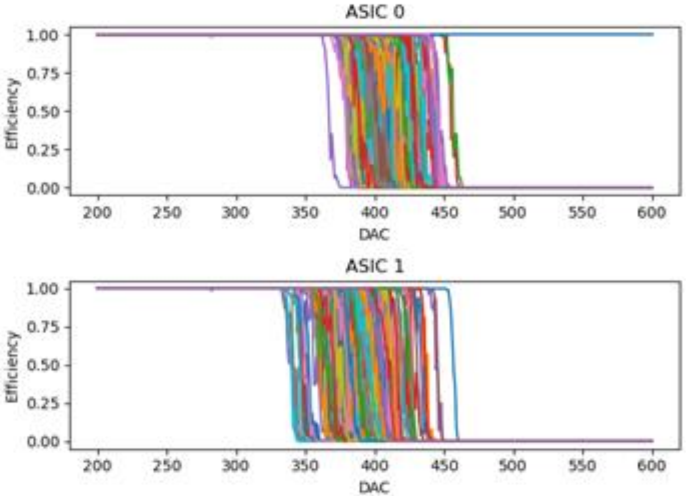
- HV OFF
  - Inject known charges (Q_inj = 12 & 36 DAQU). Data Acquisition Unit (DAQU) is a unit of charge injection.
  - Perform a V_th scan (threshold scan) → measure response.
  - Use the difference between the two scans to detect disconnected or weak bumps.
- Tune module
  - Use V_thc (threshold calibration) to align the module response.
  - Perform a charge scan → obtain Time-Over-Threshold (TOT).
- HV ON
  - Apply sensor bias to enable full depletion (charge collection).
  - Repeat V_th scan with Q_inj = 12 DAQU.
  - Compare to HV OFF scan → confirms if signal collection improves as expected.



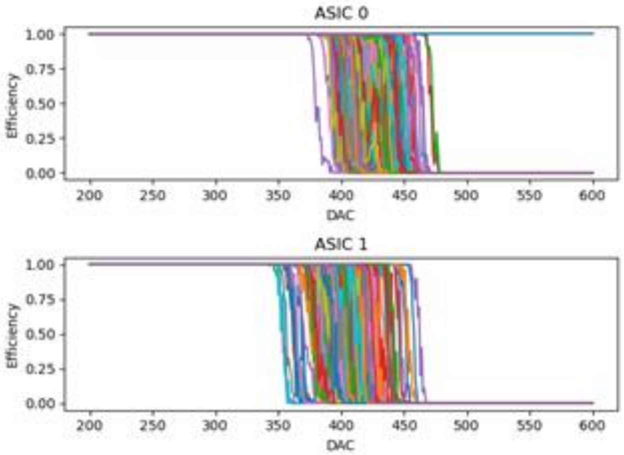
Threshold Scans for both HV on & off



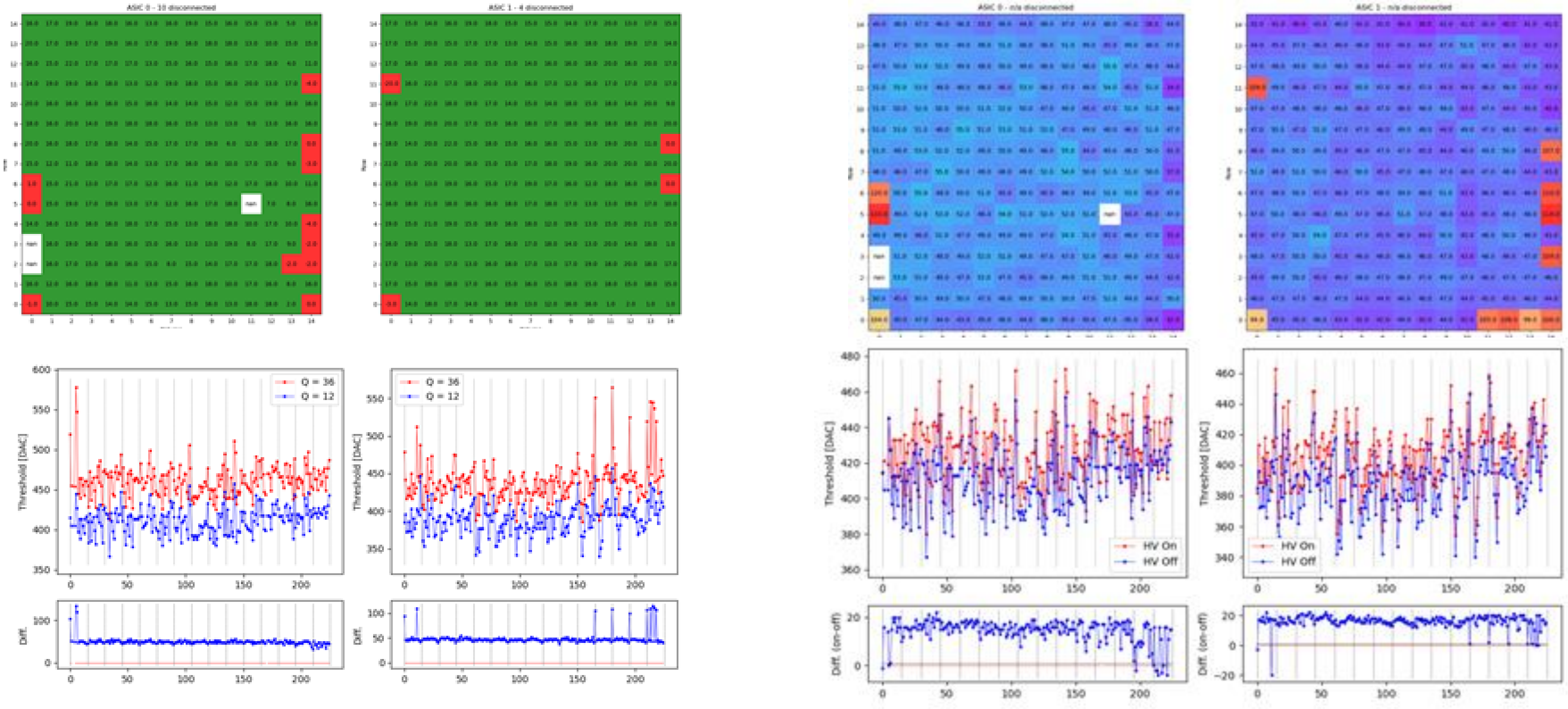




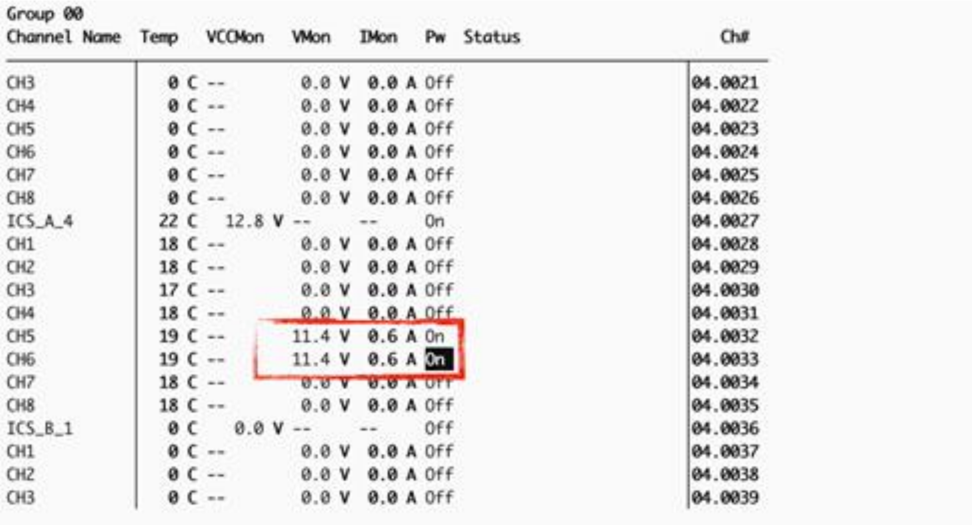
HV :Left → Off
Right → On



Bump Connections plots



Power test: Low Voltage (LV) and High Voltage (HV) DCS



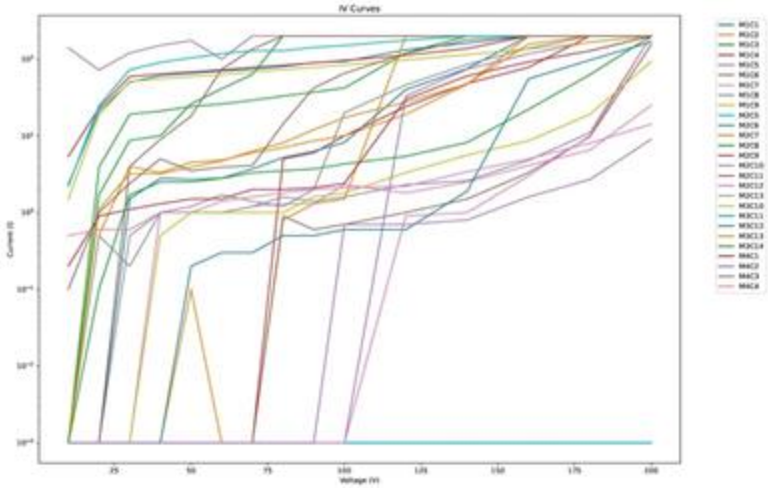
Group 00

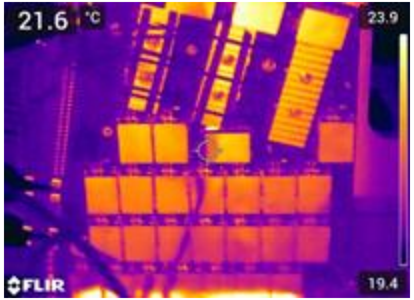
Channel Name	Temp	VCCMon	VMon	IMon	Pw	Status	Ch#
CH3	0 C	--	0.0 V	0.0 A	Off		04.0021
CH4	0 C	--	0.0 V	0.0 A	Off		04.0022
CH5	0 C	--	0.0 V	0.0 A	Off		04.0023
CH6	0 C	--	0.0 V	0.0 A	Off		04.0024
CH7	0 C	--	0.0 V	0.0 A	Off		04.0025
CH8	0 C	--	0.0 V	0.0 A	Off		04.0026
ICS_A_4	22 C	12.8 V	--	--	On		04.0027
CH1	18 C	--	0.0 V	0.0 A	Off		04.0028
CH2	18 C	--	0.0 V	0.0 A	Off		04.0029
CH3	17 C	--	0.0 V	0.0 A	Off		04.0030
CH4	18 C	--	0.0 V	0.0 A	Off		04.0031
CH5	19 C	--	11.4 V	0.6 A	On		04.0032
CH6	19 C	--	11.4 V	0.6 A	On		04.0033
CH7	18 C	--	0.0 V	0.0 A	Off		04.0034
CH8	18 C	--	0.0 V	0.0 A	Off		04.0035
ICS_B_1	0 C	0.0 V	--	--	Off		04.0036
CH1	0 C	--	0.0 V	0.0 A	Off		04.0037
CH2	0 C	--	0.0 V	0.0 A	Off		04.0038
CH3	0 C	--	0.0 V	0.0 A	Off		04.0039

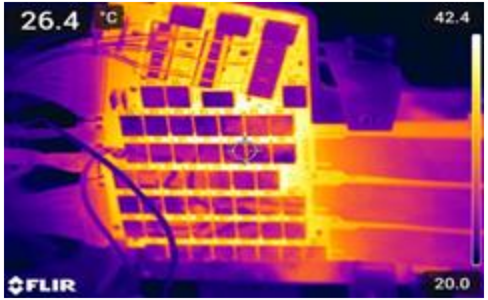
- ❑ Integration of HV to DCS fully operational enabling remote use, can operate all 54 modules, change over current protection, voltages,

Power test

- Current and voltage curves are for different modules.
- All modules were connected and powered on, to validate and check tripping point for each module.
- Over current protection tripping was set at 200 μA



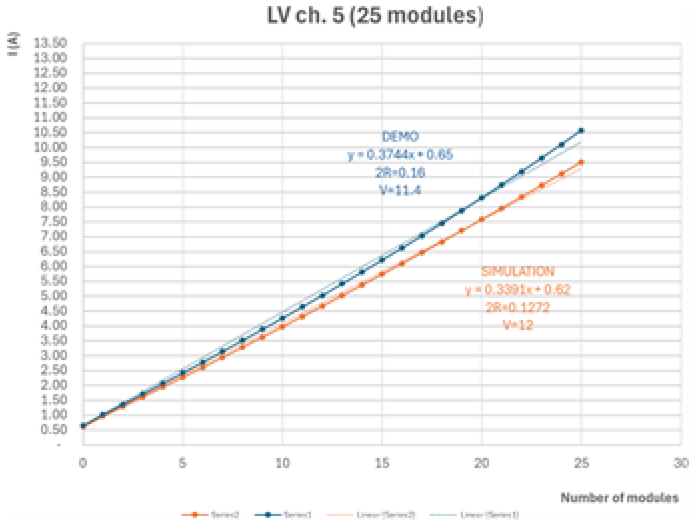


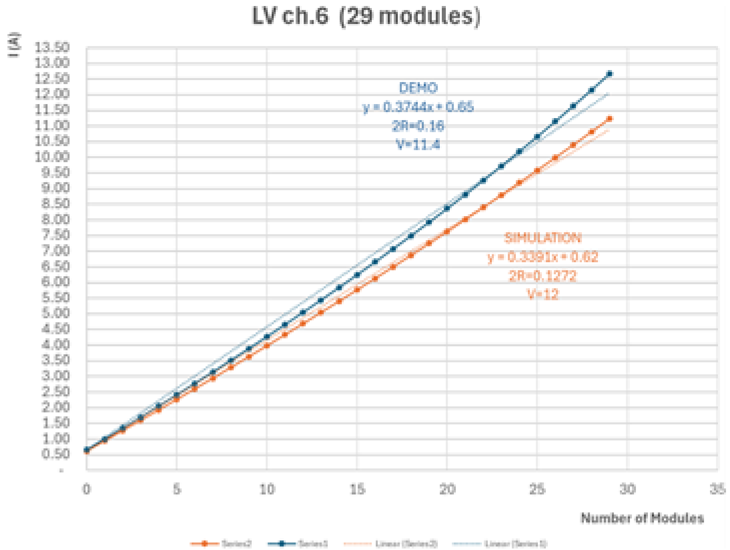


Before the modules were switched , temperatures ranged from 19.4 - 23.9 ℃

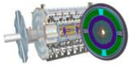
Temperature when all modules were switched on, went to around 42.4 ℃

Power Test





Two different the voltages are used for simulation 12 V and on the demonstrator 11.4 V and resistance for simulation 0.1272 Ω and on the demonstrator 0.16 Ω.We expect an increase in the LV current of ~ 0.37A per module and a total of 10.6 A in LV channel 5 (25modules) and 12.7 A in LV channel 6 (29 modules).

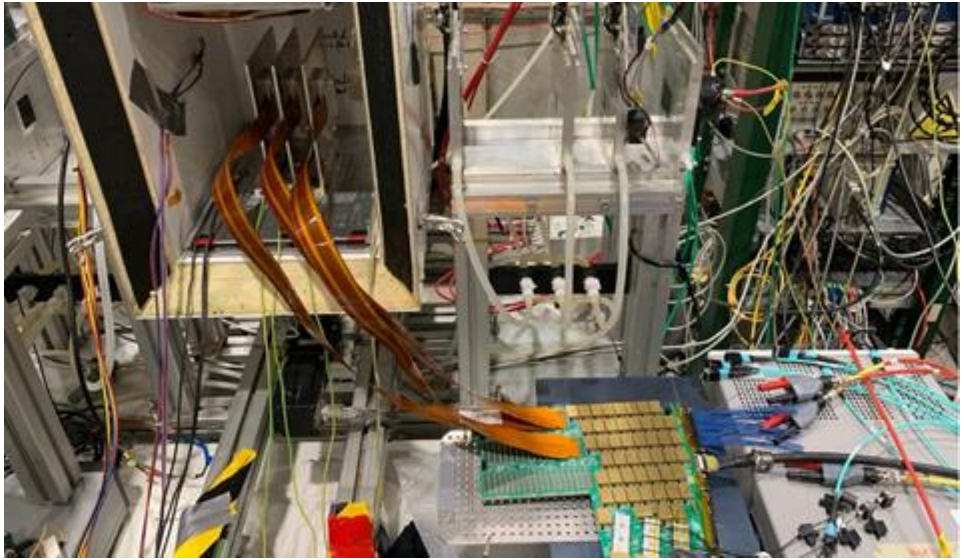


Testbeam studies

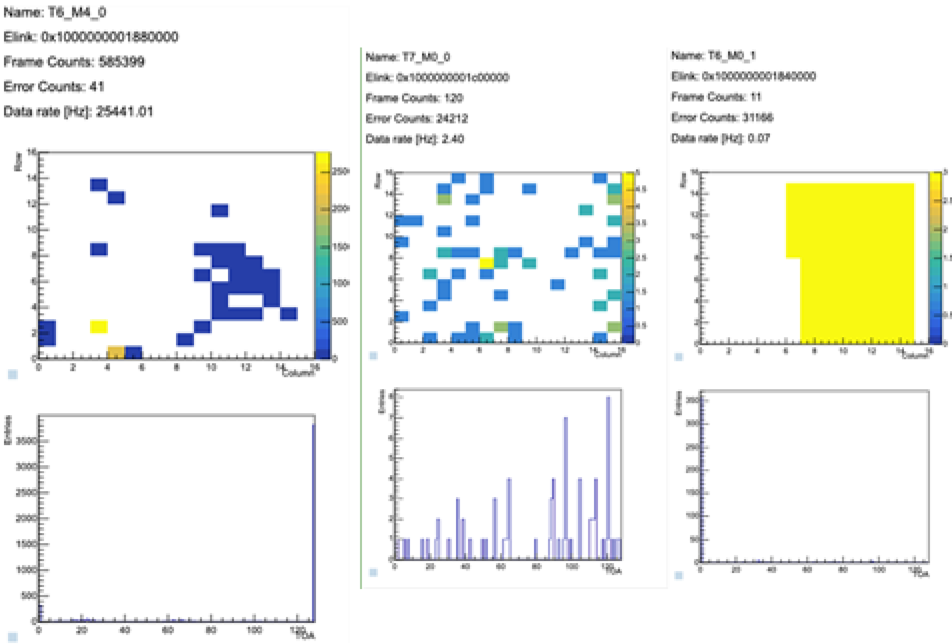
Purpose: Planned to perform testbeam with FELIX readout -> ultimately to crosscheck time resolution performance when using full electronics chain

Setup: 3 modules connected with long flex tails cables, connected to 1280 Mbps positions on the PEB

Observations: Alignments tests were successful, configuration lpGPT was successful but configuration to Altiroc was problematic



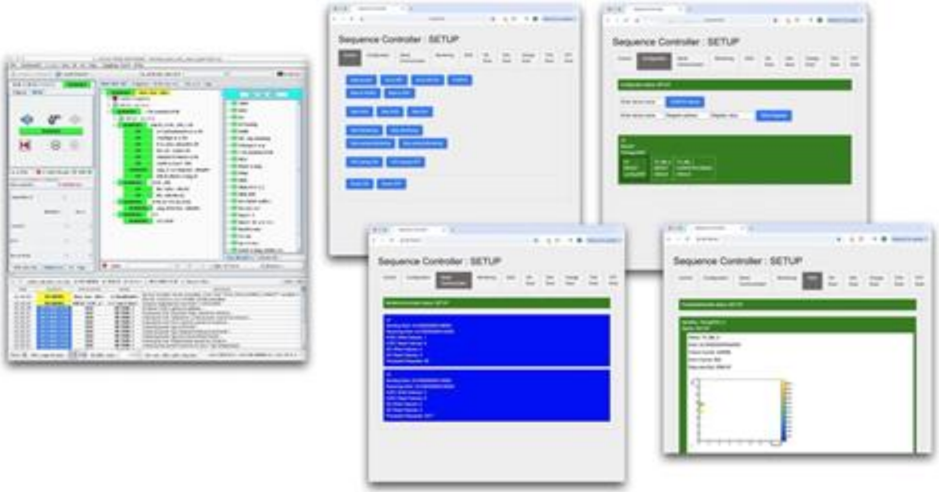
Testbeam studies

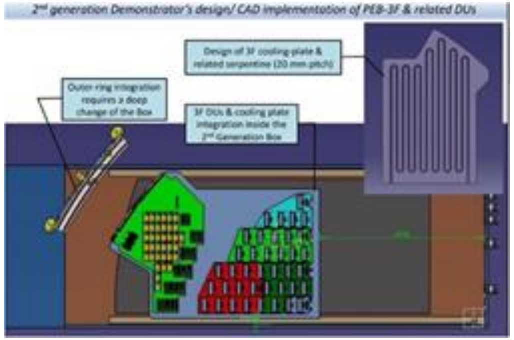


In cases where Altiroc went through we experienced lots of errors, more tests are required with the PEB to deal with such issues in future.

Recent developments in demonstrator

- ❑ DAQ software has been introduced to assist in automating some of the tests → improves efficiency
- ❑ 2nd generation demonstrator with Faraday cage is currently being developed





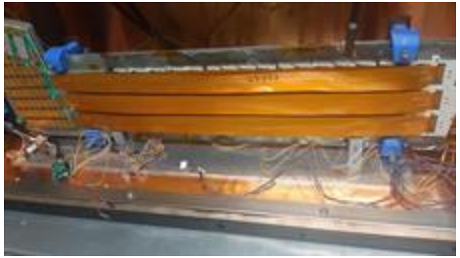
Summary and outlook

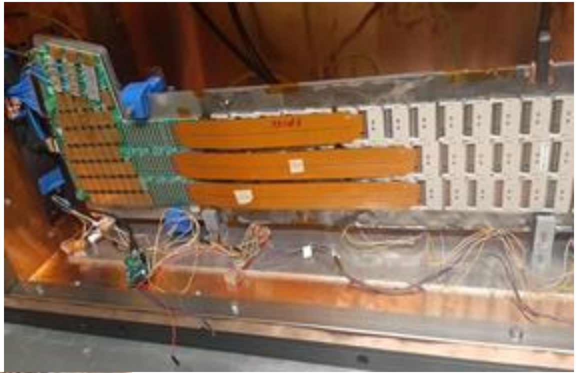
- ❑ The LV, HV, and interlock systems are now integrated into the demonstrator
- ❑ All functional modules can be operated with DAQ software
- ❑ Read the temperature of the bPOLs on the PEB, one of the action items from the PEB-FDR
- ❑ The alignment issue appears to be caused by several source FELIX, fibre, LpGBT
- ❑ With new DAQ software all measurements will be done on the demonstrator to validate its functionality

Kea Leboha! Pula Nala!

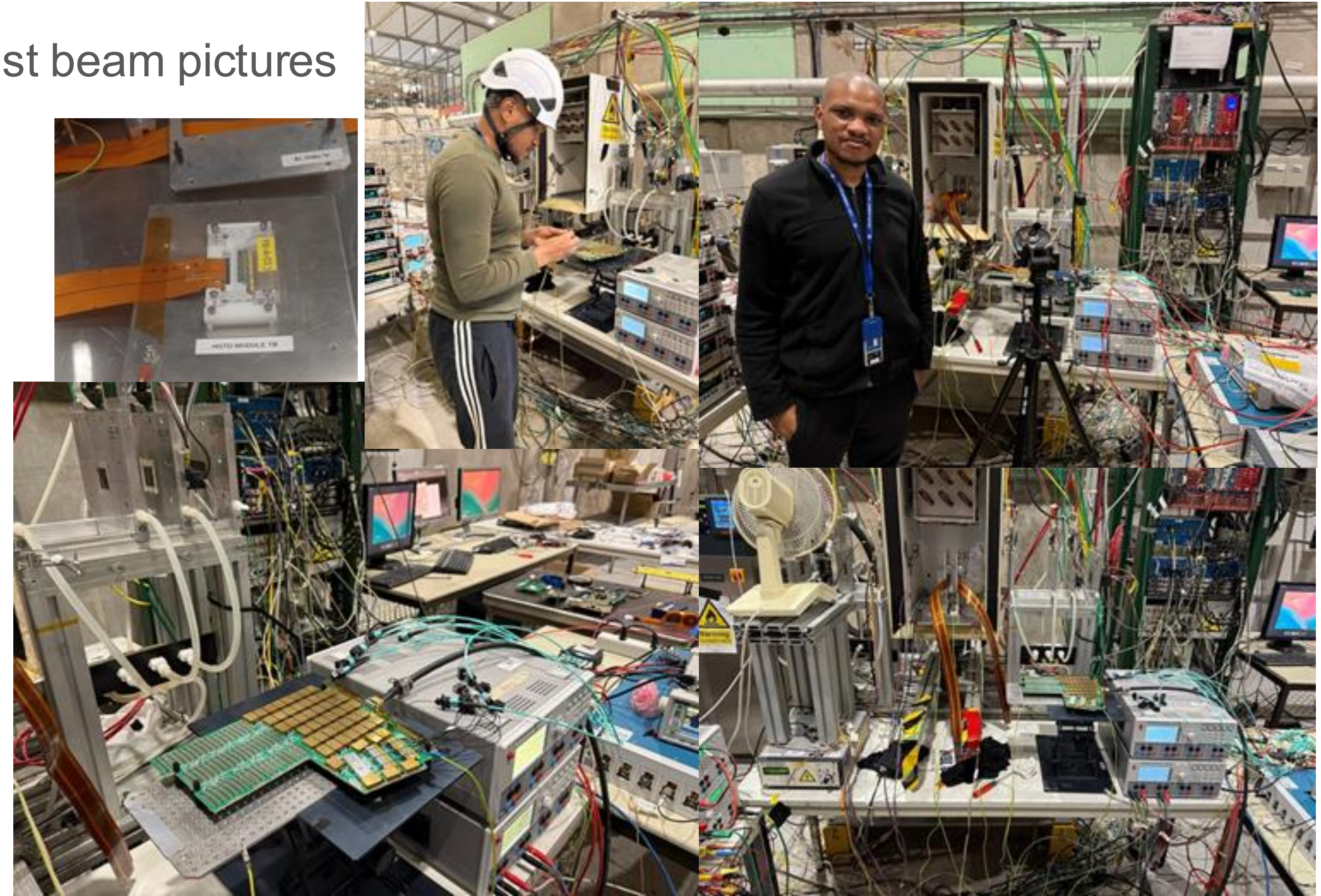
BACK UPS

Demonstrator pictures





Test beam pictures



Detector Unit modules

- Scheme of three HGTD modules attached to the cooling plate (in blue).