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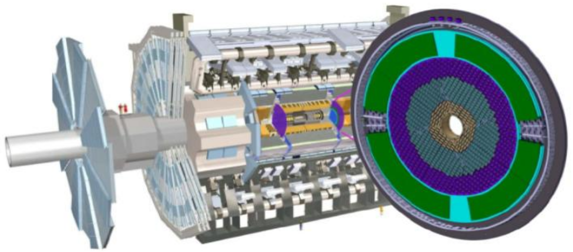


ATLAS EXPERIMENT

Overview of the status of the High Granularity Timing Detector for the ATLAS phase 2 upgrade

Rachid Mazini

Mukesh Kumar, Thabo Lepota, Katlego Machethe

Wits University

Outline

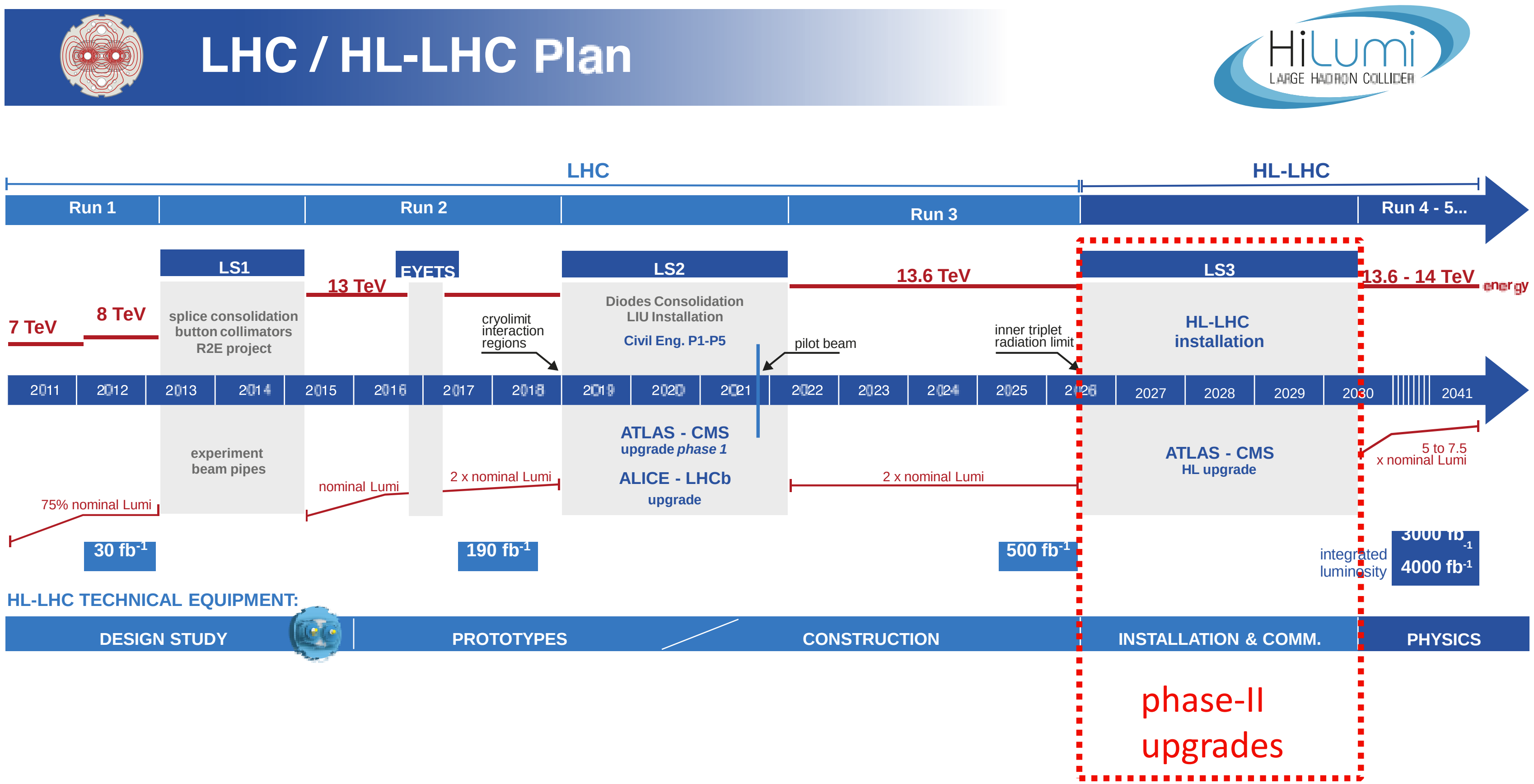
- Motivation for timing in the future ATLAS detector
- HGTD timing-detector concept
- Overview of LGADs and ALTIROC
- HGTD module assembly, Disks, Vessels
- Involvement of Wits/ICPP in HGTD

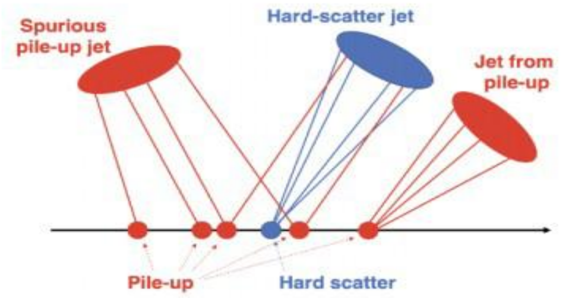
High Luminosity LHC

High Luminosity LHC (HL-LHC):

- **Upgrade** of the Large Hadron Collider, enhancing beam intensity, emittance and final focus
  → increase of the instantaneous luminosity by factor **~4** up to 7.5×10^{34} $cm^{-2}s^{-1}$
- Leads to more challenging data-taking conditions for the experiments: **event pile-up, radiation damage**
- HL-LHC installation and upgrades of the LHC detectors during long shutdown **2026-2030**

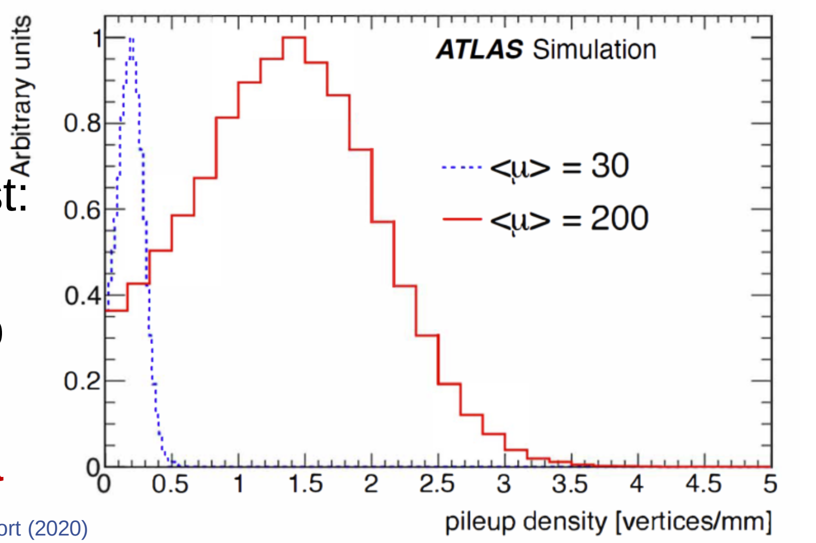
https://hilumilhc.web.cern.ch/content/hl-lhc-project



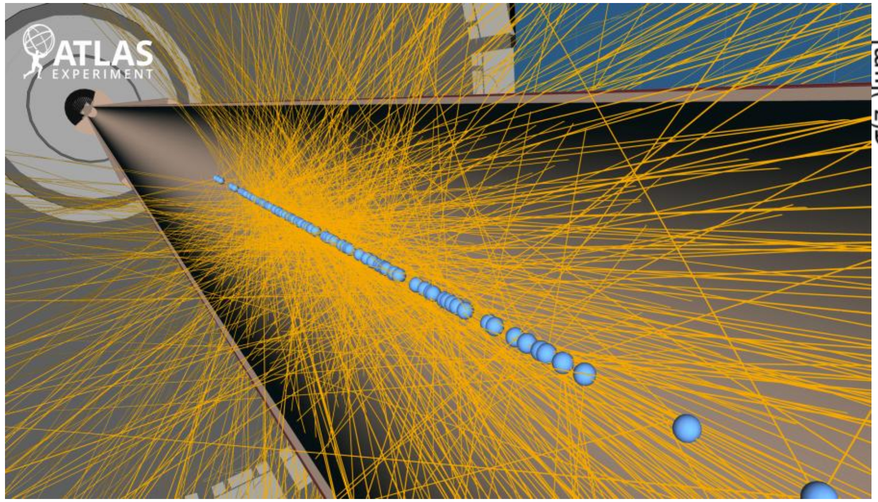


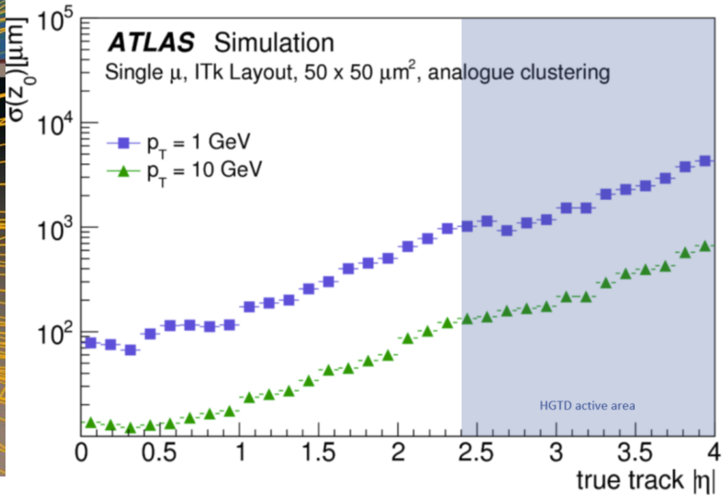
ATLAS detector challenges at HL-LHC

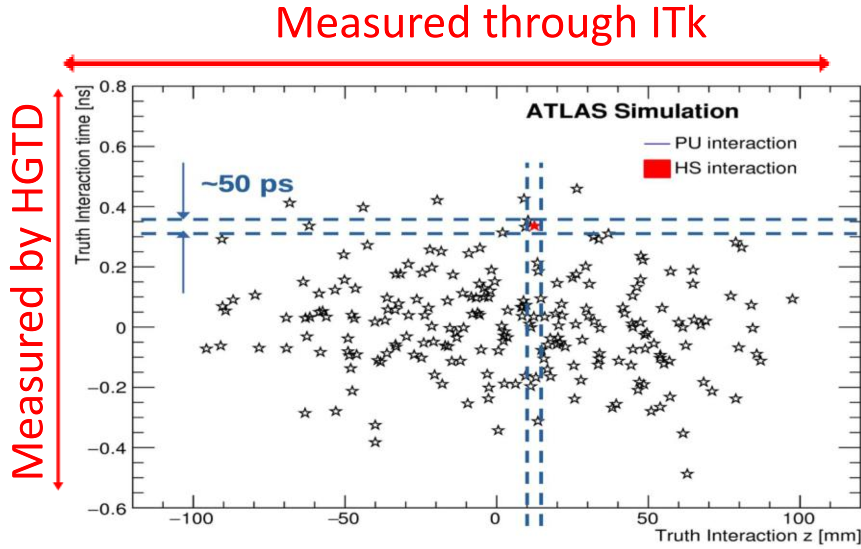
- Expected **pile-up** in the ATLAS detector: <μ> = **200** interactions per bunch crossing (on average 1.6 vertices/mm)
- Highest rates in **forward detector regions**, where tracker resolution is poorest: correct assignment of tracks to vertices becomes challenging
- Adding **precision-timing information** in the forward regions improves pile-up rejection and vertex reconstruction
- With 50 ps MIP time resolution, the pile-up suppression is expected to improve by **a factor of ~ 6**



Plots: HGTD Technical Design Report (2020)
https://cds.cern.ch/record/2719855/

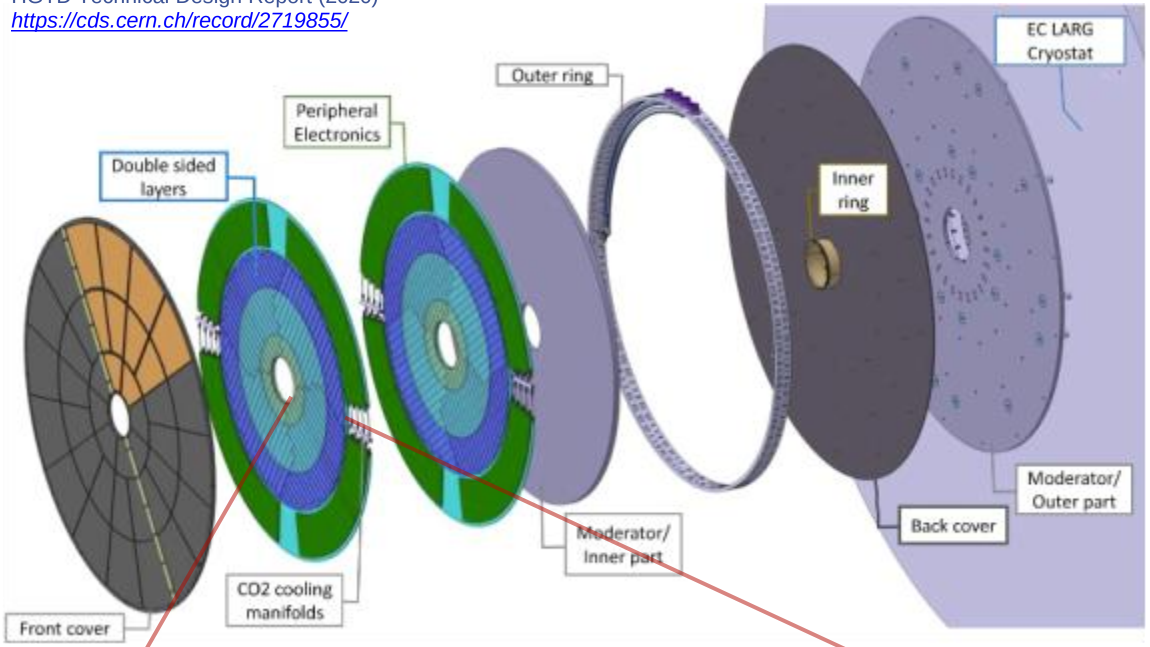


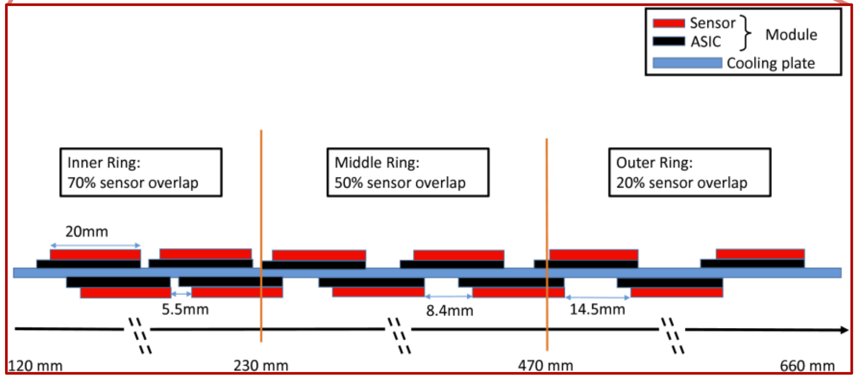


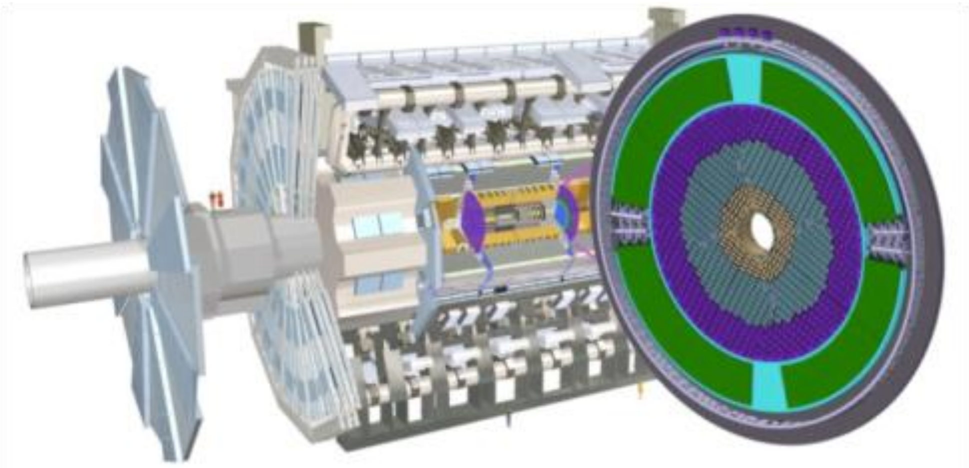


High Granularity Timing Detector

HGTD Technical Design Report (2020)
https://cds.cern.ch/record/2719855/





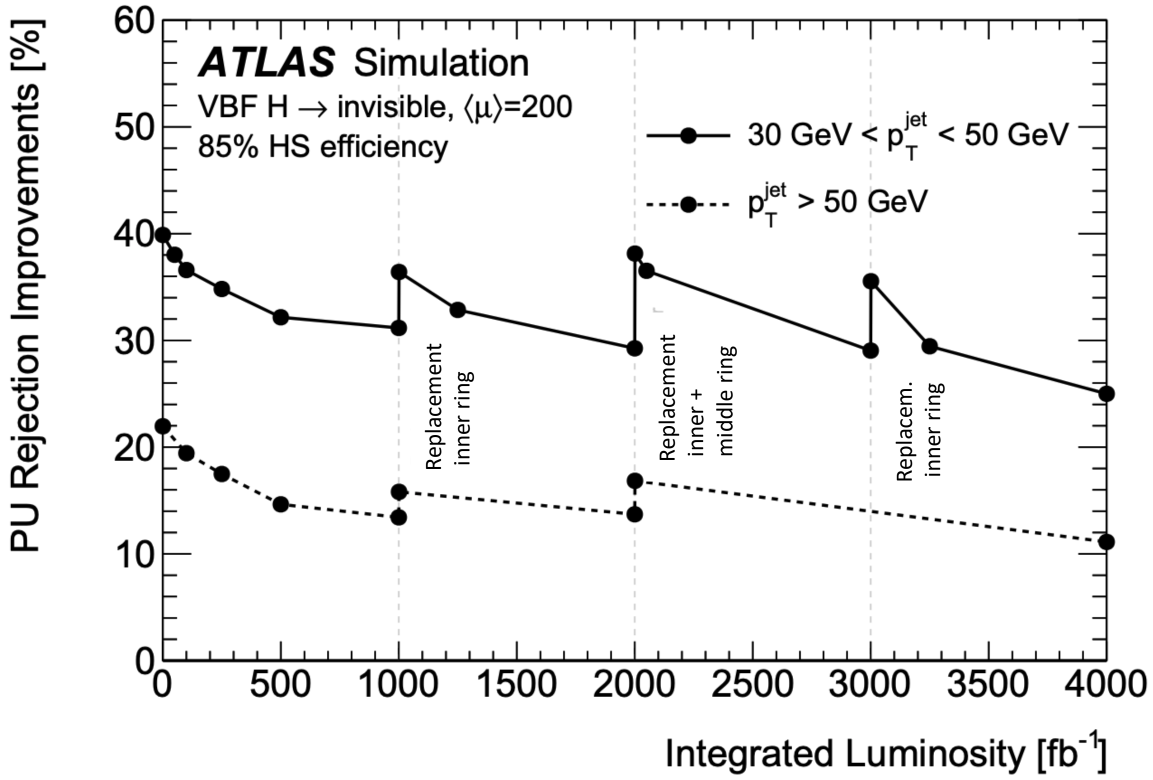


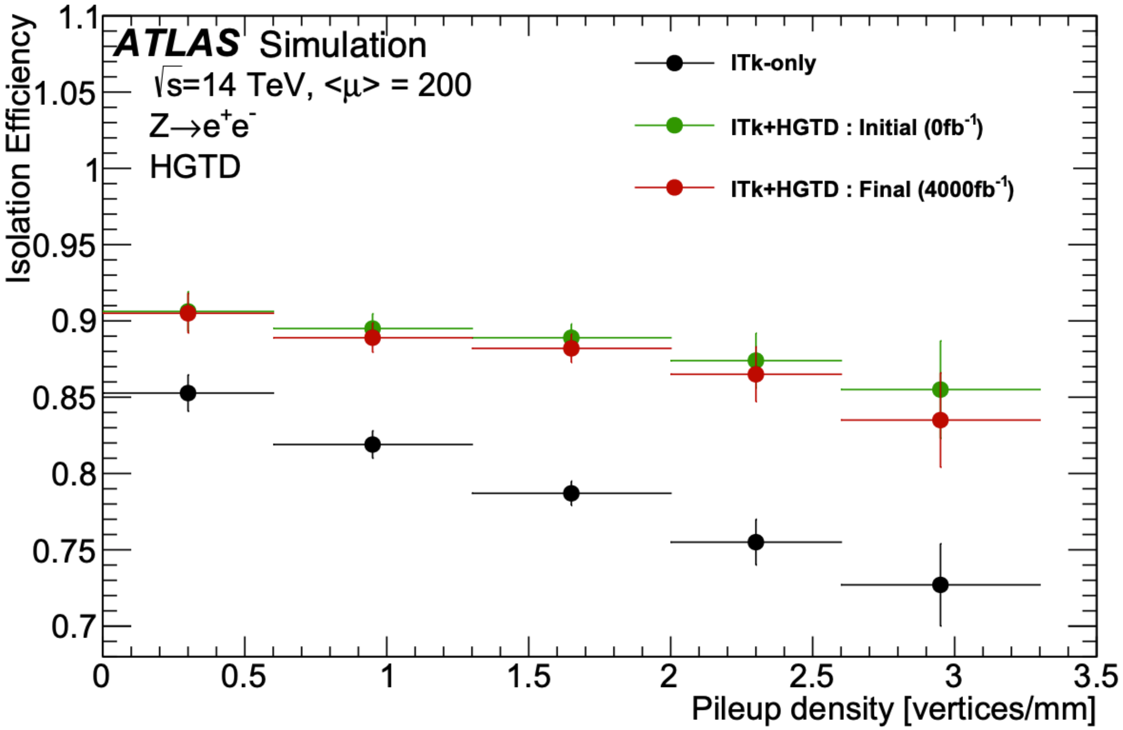
High Granularity Timing Detector (HGTD):

- Placed between Inner Tracker (ITk) and Liquid Argon Calorimeter
- Active area coverage: **2.4 < |η| < 4.0**
- Consists of **8032** modules (2 LGAD sensors + 2 r/o ASICs each) **6.4 m²** of silicon sensors
- Radiation hardness requirements (with replacements of the **inner (every 1000 fb)** and **middle (every 2000 fb)** rings):
  - Maximum fluence: $\mathbf{2.5\times10^{15}\ n_{eq}/cm^2}$; TID: 2 MGy
- Operating temperature **-30ºC** (CO_2 dual phase cooling)
- Two instrumented double layers per side
- Overlap between modules on all rings
- Track-time resolution: **35 ps** (start) - **50 ps** (end)

Performance improvement with HGTD

HGTD Technical Design Report (2020)
https://cds.cern.ch/record/2719855/





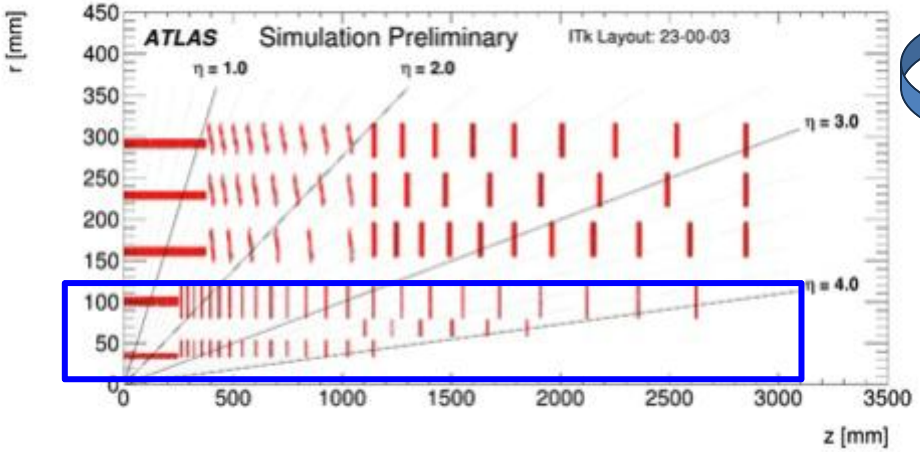
- Track-timing information from HGTD will allow for recovering the performance in the forward detector regions:
  - Improved rejection of **pile-up**
  - Increased **lepton-isolation** efficiency
- HGTD also allows for measuring the **luminosity** bunch-by-bunch (hit counting at 40 MHz), <1% accuracy

Improvement in track and Vertex reconstruction

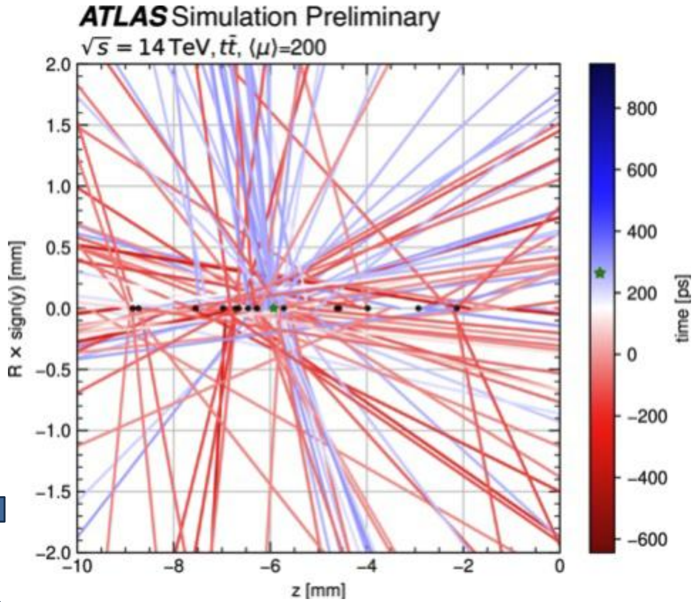
After 2 ab^{-1}, two innermost layers of ITk will be replaced

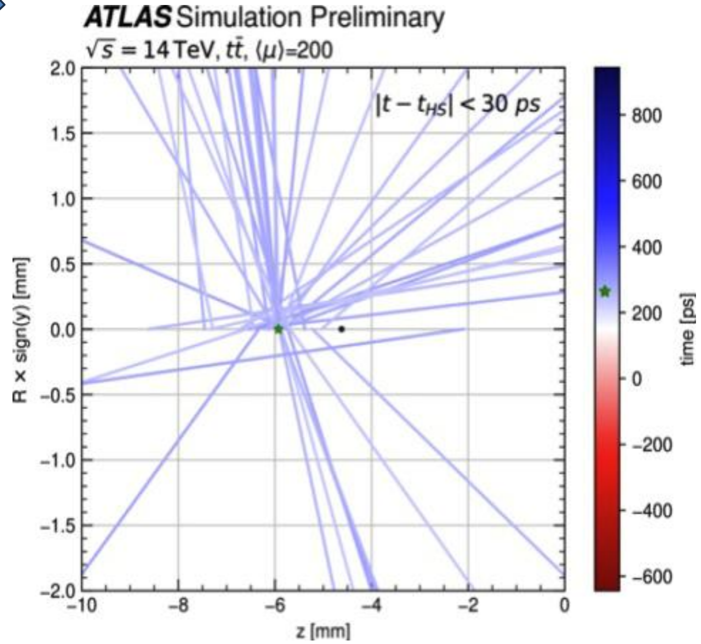
⇒ Opportunity to include a 4-dimensional (4D) tracker in the central region capable of measure simultaneously spatial and temporal coordinates

ITk pixel

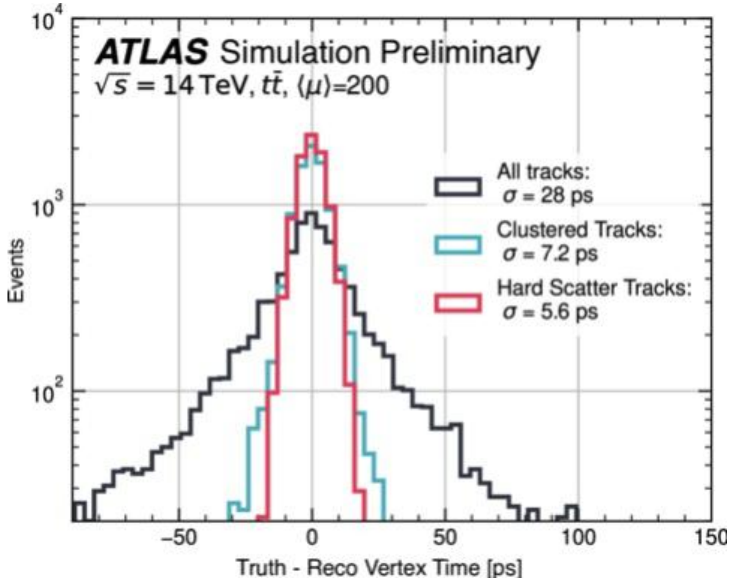


ATL-PHYS-PUB-2022-047



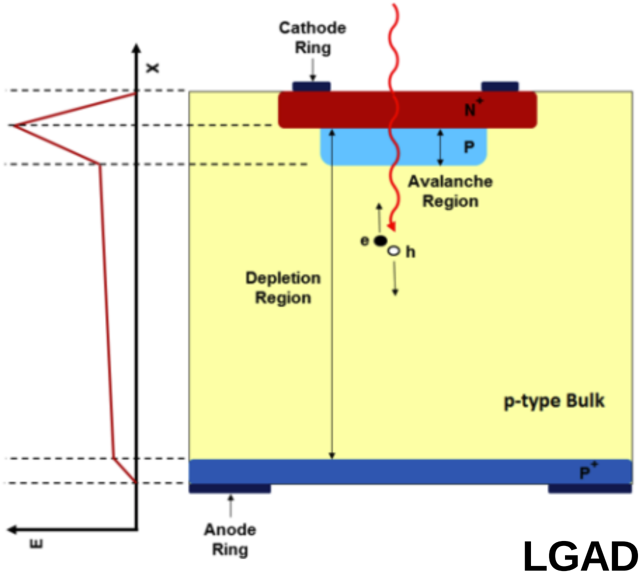


- Time of the primary vertex can be reconstructed using also central tracks
- Resolution down to 7.2 ps with single track resolution of 30 ps



The HGTD LGAD Sensors

- **Low Gain Avalanche Diod (LGAD)** technology used for HGTD **15×15 pads**
- Pad size: **1.3 mm×1.3 mm**
- **3.6 M** channels
- Physical / active thickness: **775 µm / 50 µm**
- **~22k** sensors to be produced



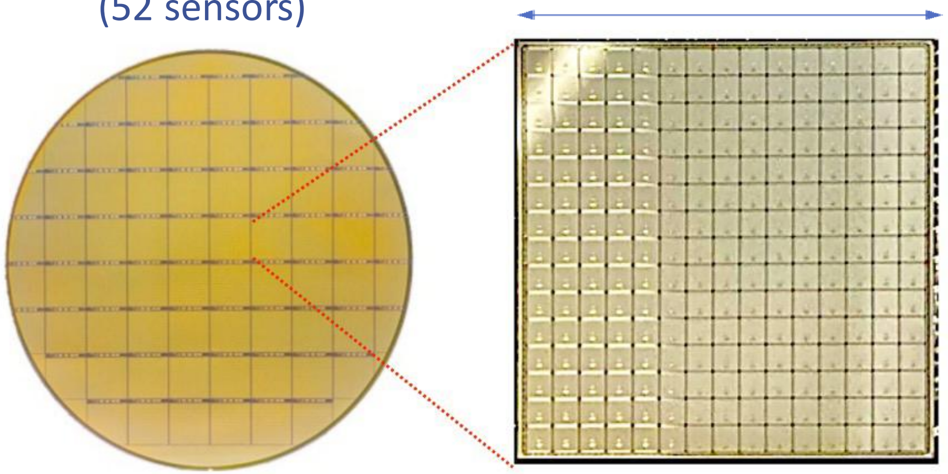
LGAD Technology:

- n-on-p sensor with p-type mult. layer
- extra p-type **gain-layer** for moderate gain 10-40

→ Fast **rise time** and larger **signal-to-noise** ratio

→ Excellent time resolution

8” sensor wafer
(52 sensors)



LGAD sensors requirements:

- Hit-time resolution: **40 ps** (start) - **70 ps** (end)
- Collected charge per hit: **10 fC** (start) - **4 fC** (end)
- Hit efficiency: **97 %** (start) - **95 %** (end)

Time resolution: $$\sigma^2_{\text{det}} = \sigma^2_{\text{Landau}} + \sigma^2_{\text{elec}}$$

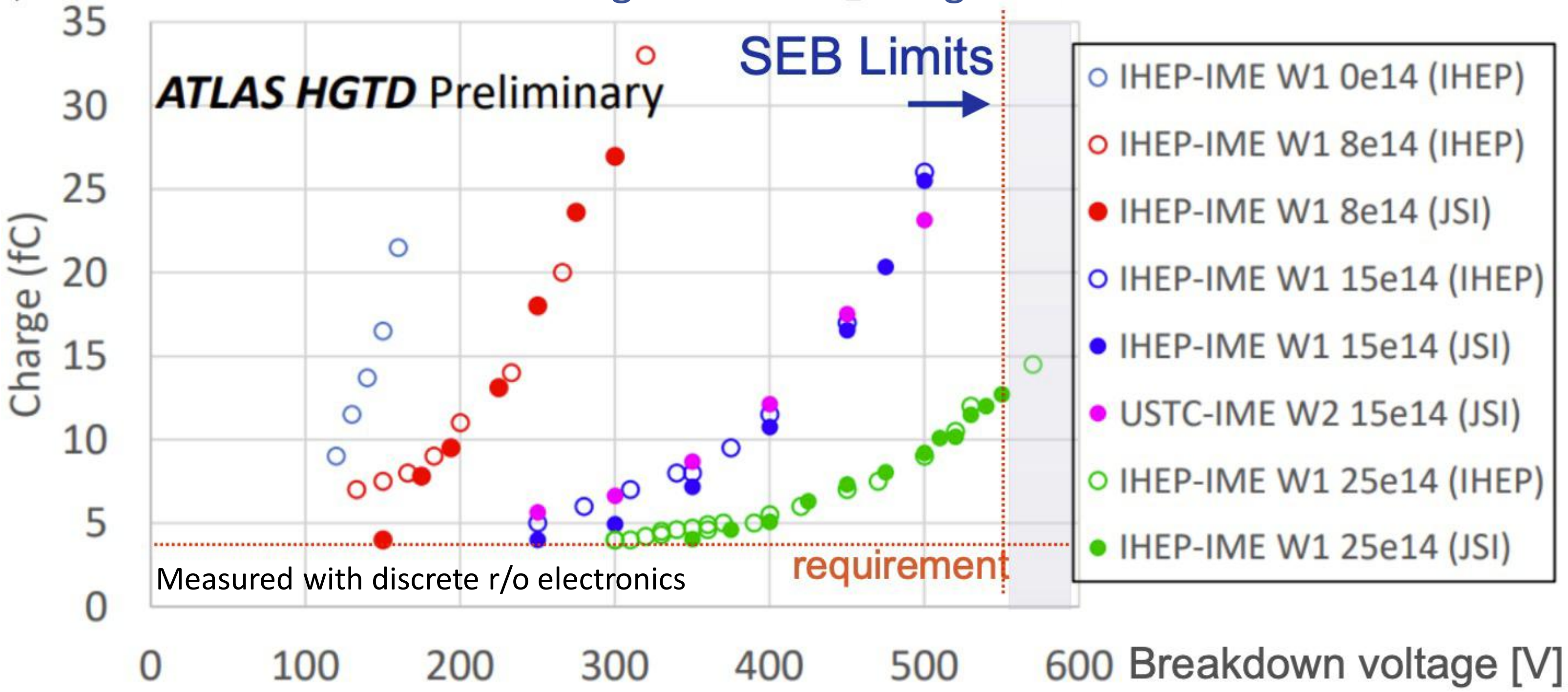
$$\sigma^2_{elec} = \left(\frac{t_{rise}}{S/N}\right)^2 + \left(\left[\frac{V_{thr}}{S/t_{rise}}\right]_{RMS}\right)^2 + \left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2$$

Jitter *Timewalk*

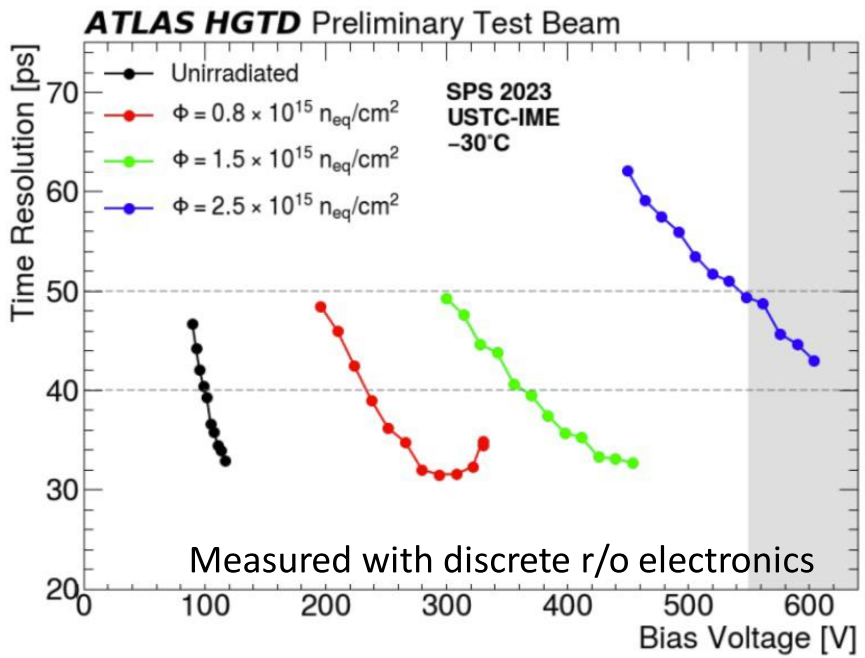
LGAD radiation effects (I)

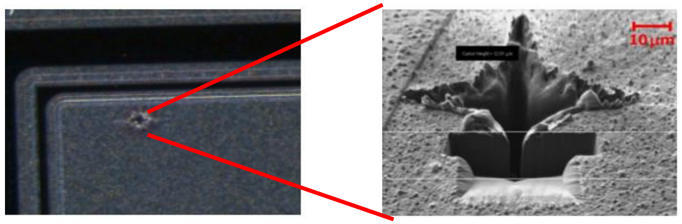
https://twiki.cern.ch/twiki/bin/view/AtlasPublic/HGTDPublicPlots

LGAD signal vs. bias voltage



LGAD time resolution vs. bias voltage

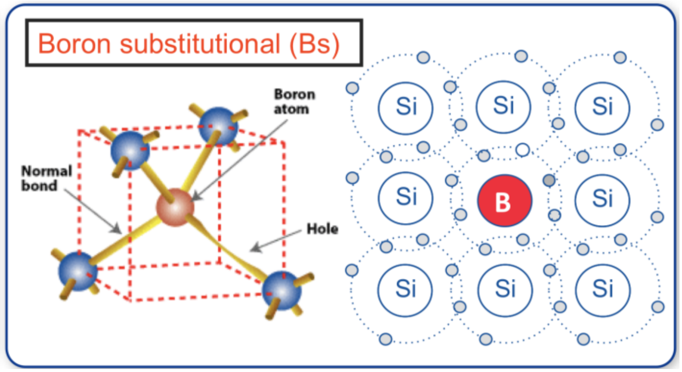




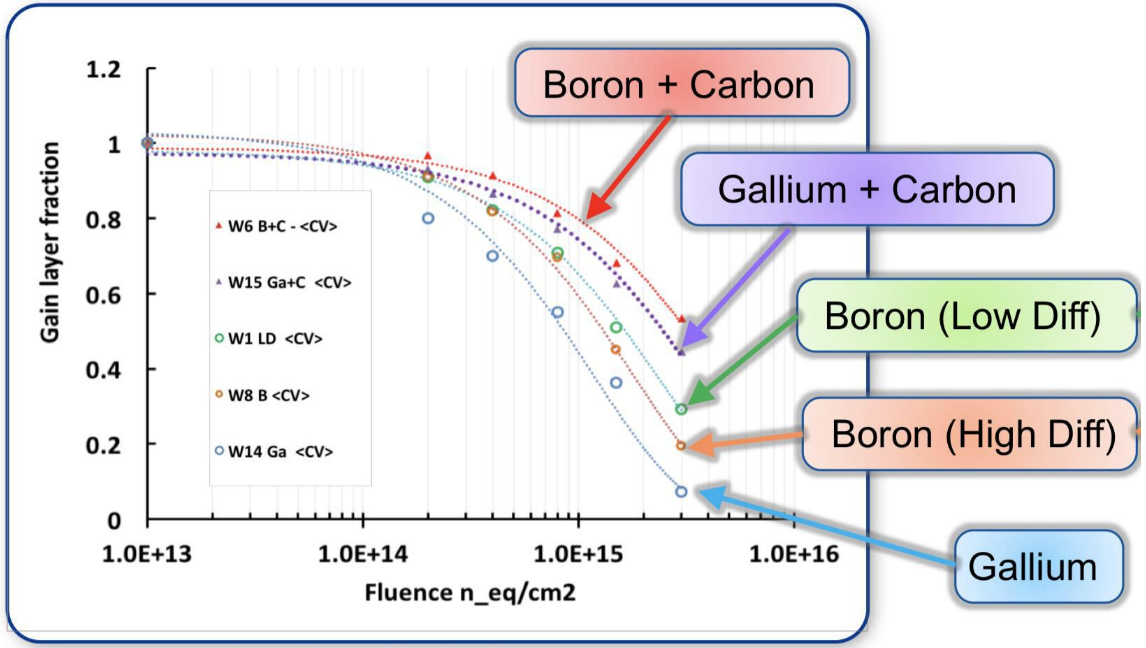
- LGAD performance degrades with radiation exposure due to a **loss of gain**
- Recovered by increasing the **bias voltage**
  - Limit imposed by *Single Event Burnout* (**SEB**) effect (local breakdown of electric field) → V_{max}~550 V for 50 μm thickness
- **Carbon enriched gain layer** to reach lower operation voltages and thereby improved radiation hardness.

LGAD radiation effects (II)

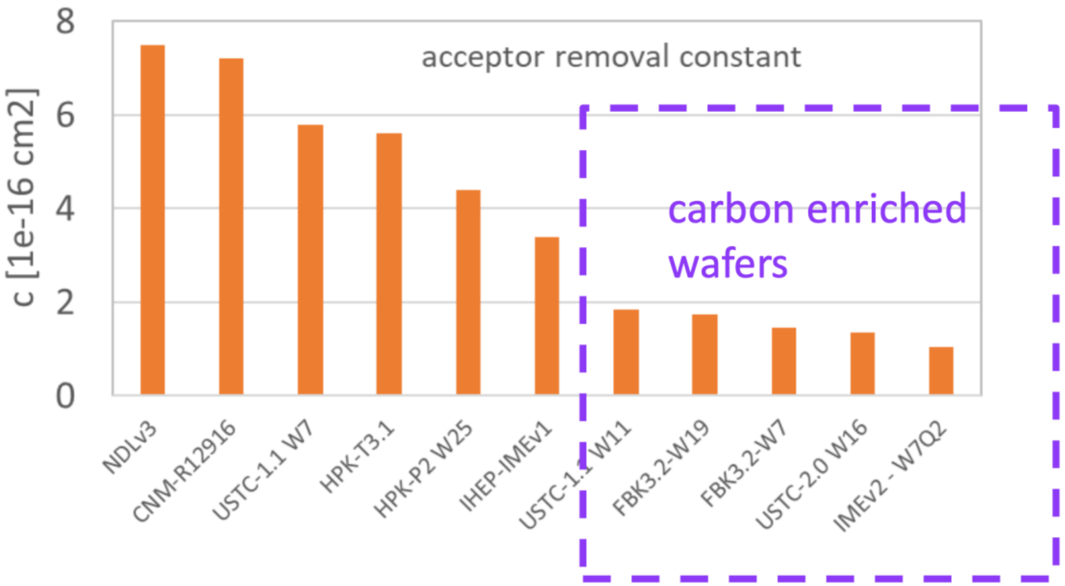
- Radiation causes boron doping in gain layer less active (acceptor removal). This can be mitigated by carbon-enriched LGAD, in which the carbon “stabilizes” the boron doping,
- The IHEP-IME/FBK/USTC-IME LGAD with carbon,
  - Lower the acceptor removal ratio,
  - Making the senor more radiation tolerant.



See CERN Detector seminar
https://indico.cern.ch/event/1088953/



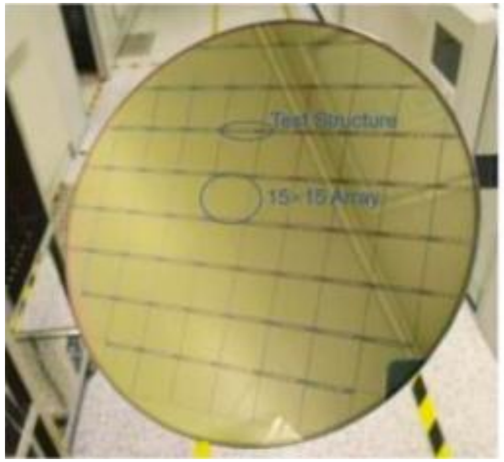
[G.Paternoster, FBK, Trento, Feb.2019]

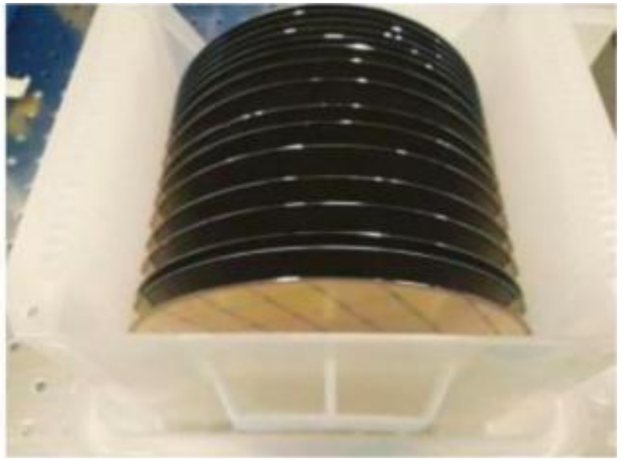


LGAD sensors preproduction

IHEP-IME

52 sensors/wafer

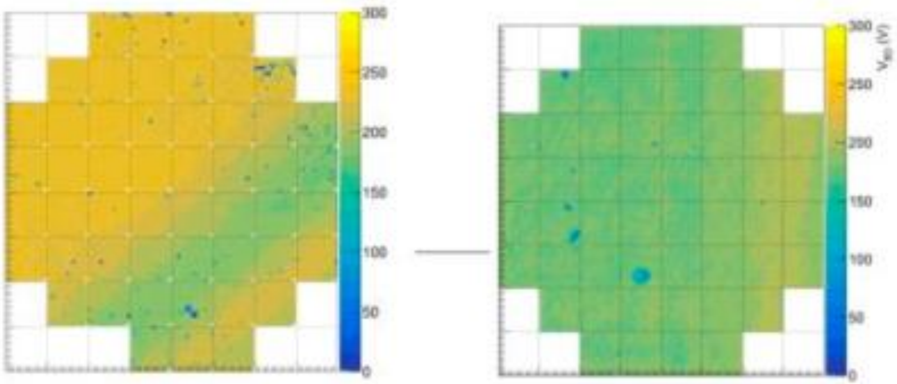




115 wafers processed (90 already fabricated)

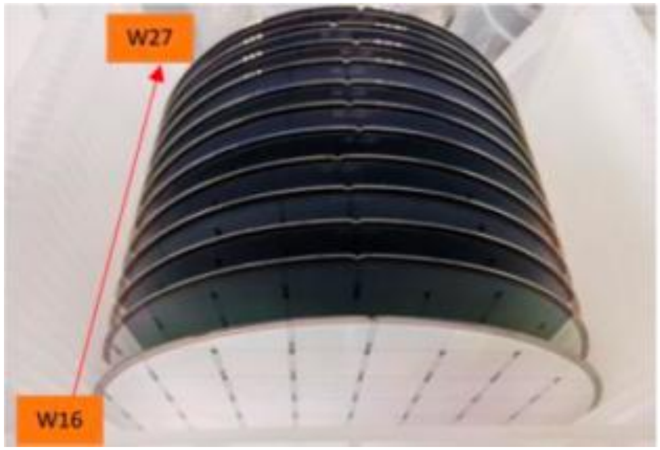
- Considering min. 35% yield → 2093 sensors
- Required: 200 (in-kind) +580 (CERN) sensors

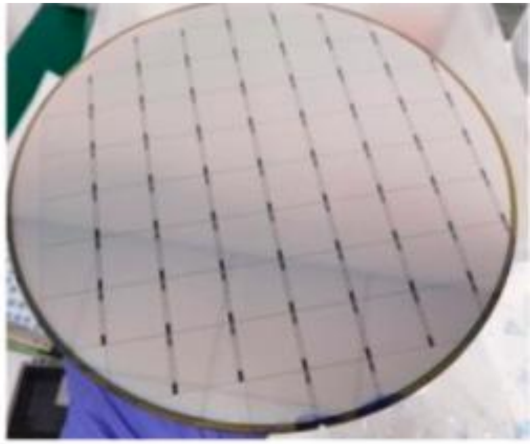
Satisfy Requirements



USTC-IME

52 sensors/wafer

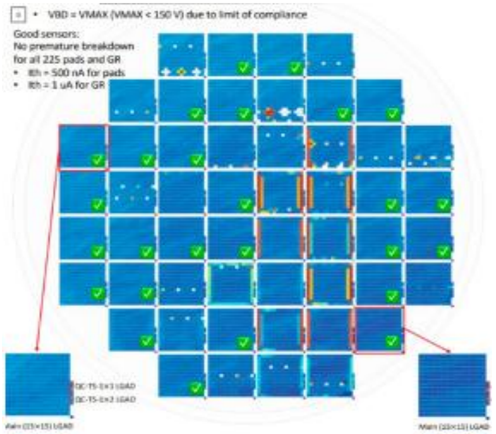




27 wafers fabricated

- Considering min. 35% yield → 590 sensors
- Required: < 200 (in-kind)

Satisfy Requirements

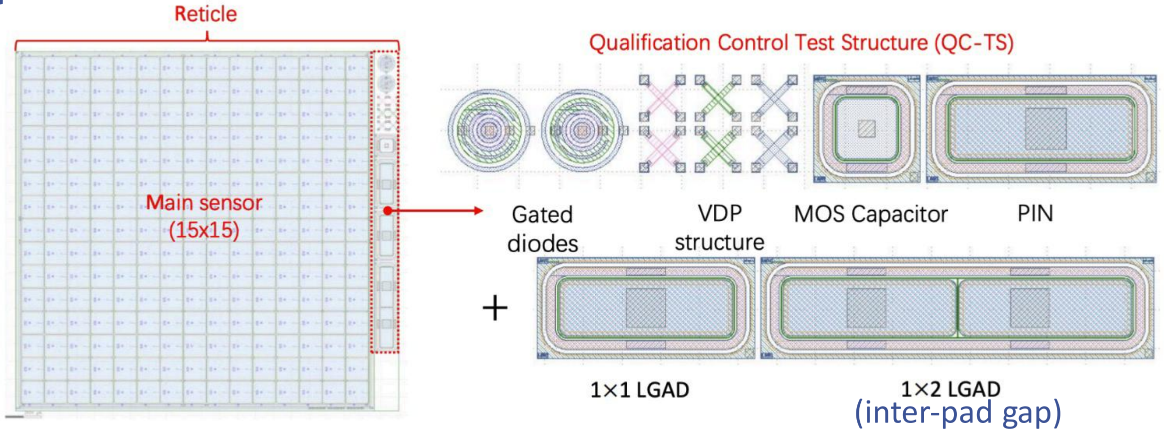


9 wafers passed all the requirements

LGAD sensor production and QC

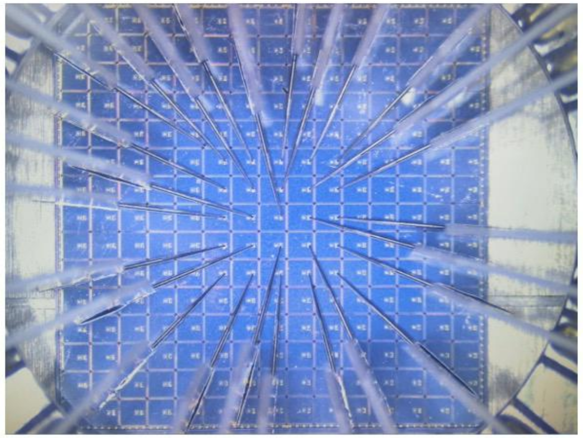
https://indico.cern.ch/event/1386009/contributions/6279120/

- Pre-series production of a total of **117** wafers (8”) (5% of main production, 1100 sensors) recently concluded
- Sensors from two vendors: **IHEP-IME** and **USTC-IME**
- Systematic electrical measurements on all **main sensors** to extract leakage currents and breakdown values
- Electrical measurements on dedicated quality-control test structure (**QC-TS**), to monitor various technological parameters
- **Irradiation tests** on main sensors and QC-TS

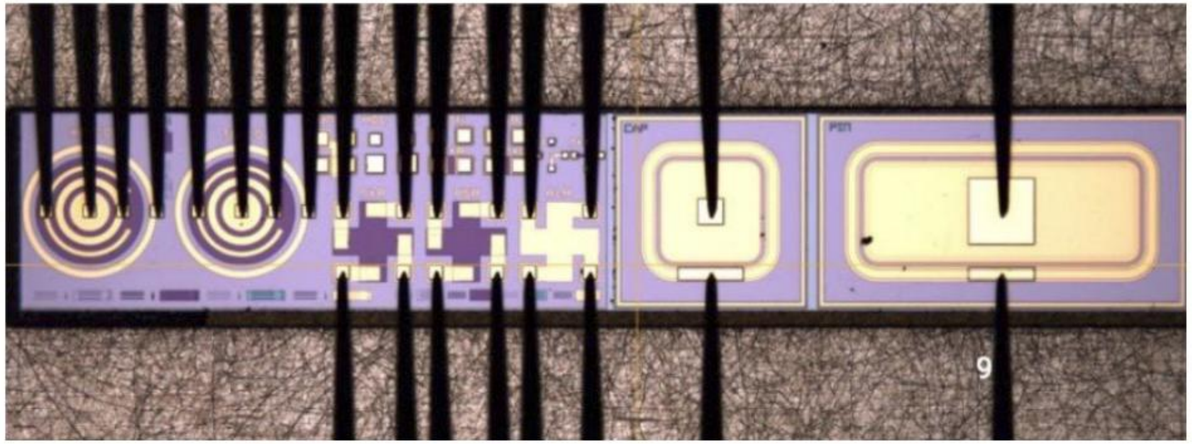


QC Device	Parameter	Description	Technique used
Single LGAD	Vgl	Gain layer depletion voltage	C-V
	Vfd	Full depletion voltage of the device	C-V
	I@Vfd	Current at full depletion voltage	I-V
	Vbd	Device breakdown voltage	I-V
	Cpad	Electrode capacitance	C-V
PIN	Vbd	Breakdown Voltage	I-V
	Ileak	Leakage Current	I-V
MOS	tox	Oxide Thickness	C-V
	Vfb	Flatband Voltage	C-V
VDP NA	R_sheet	Sheet Resistance for N implantation	I-R
VDP PS	R_sheet	Sheet Resistance for P implantation	I-R
VDP Al	R_sheet	Sheet Resistance for Aluminum	I-R

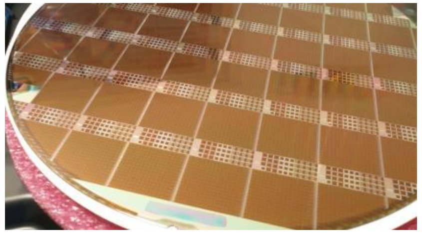
Probe-card measurement on main sensor



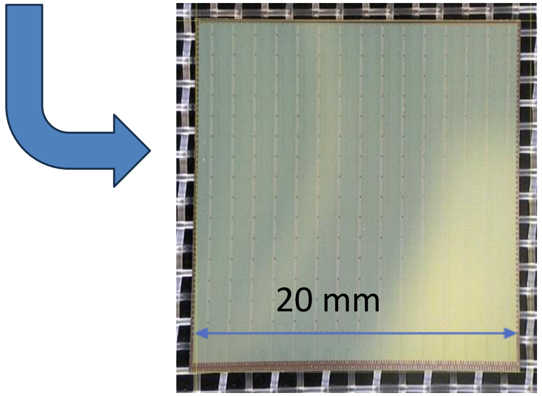
Probe-card measurement on quality-control test structure (QC-TS)



The ALTIROC readout ASIC



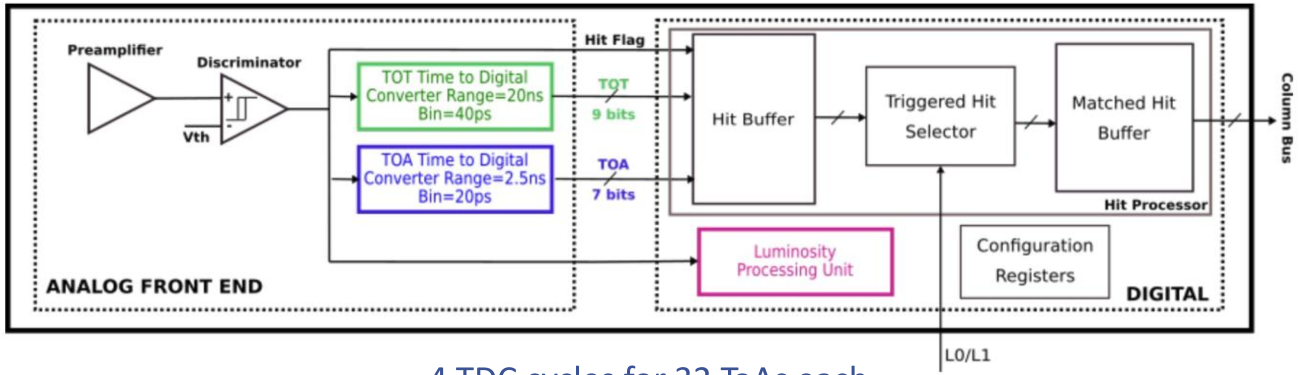
ALTIROC-A



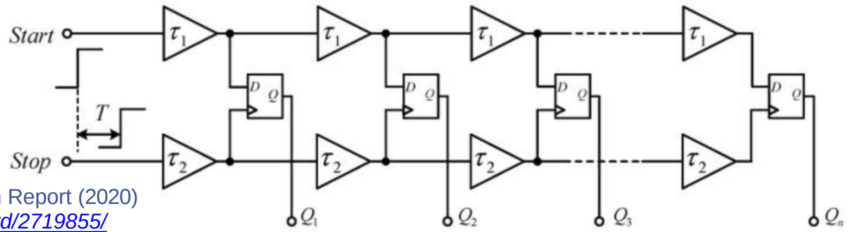
- **A**TLAS **L**GAD **Ti**ming **I**ntegrated **R**ead-**O**ut **C**hip **(ALTIROC)**
- **225 channels** matching LGAD sensor pixels
- 130 nm **CMOS** from TSMC
- Jitter: < 25 ps at 10 fC (< 65 ps at 4 fC)

- Discriminator threshold >= **2 fC**
- TDC with 20 ps binning
- Provides Time-Of-Arrival (**TOA)** and Time-Over-Threshold (**TOT)** information
- Final version: **ALTIROC-A** (under test)
- Radiation hard up to 2 MGy

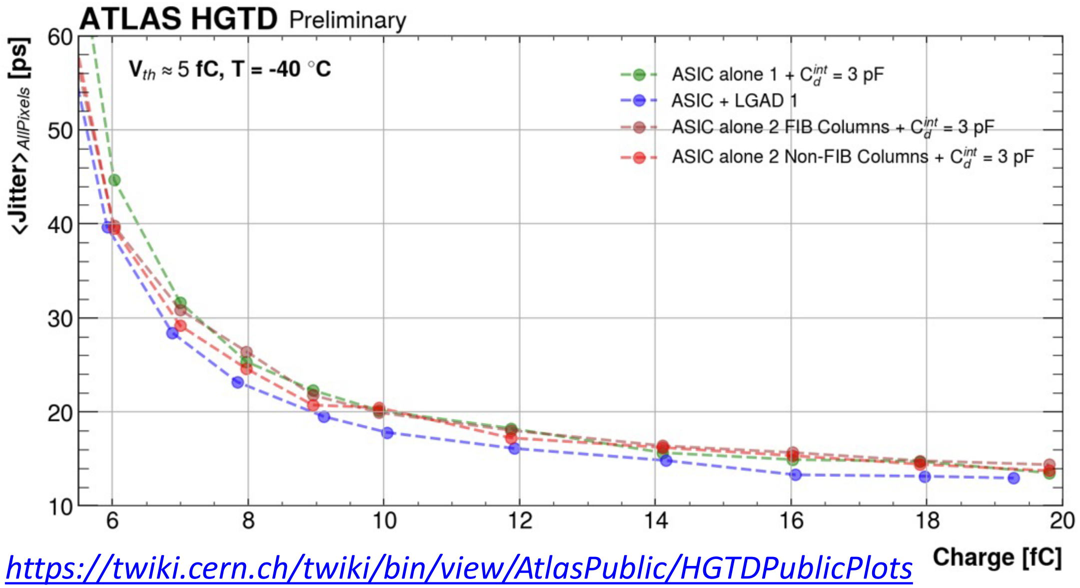
ALTIROC architecture



4 TDC cycles for 32 ToAs each



Jitter vs. charge for ALTIROC-A, detection threshold: 5 fC



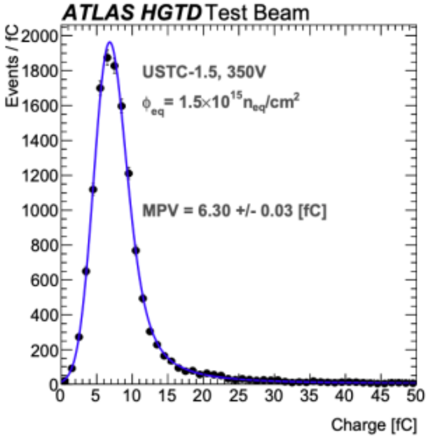
HGTD Technical Design Report (2020)
https://cds.cern.ch/record/2719855/

https://twiki.cern.ch/twiki/bin/view/AtlasPublic/HGTDPublicPlots

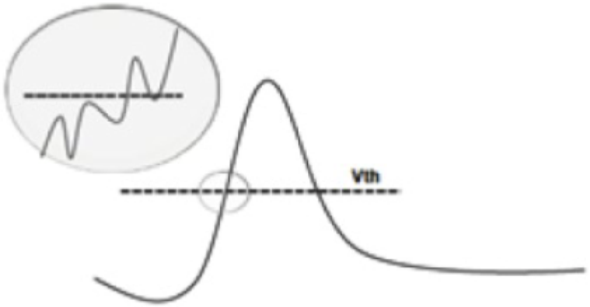
Contributions to timing accuracy

$$\sigma^2_{total} = \underbrace{\sigma^2_{Landau}}_{\text{sensor}} + \overbrace{\sigma^2_{Timewalk} + \sigma^2_{Jitter} + \sigma^2_{TDC} + \sigma^2_{Clock}}^{\text{read-out electronics}}$$

- **Landau Contribution:**
  Fluctuations of energy deposition + charge transport in the sensor
  → Mitigation: Small sensor active thickness (50 µm), saturated drift velocity
  → $\boldsymbol{\sigma_{Landau} \gtrsim 25}$ **ps**



- **Jitter:**
  Due to electronics noise in the signal shape
  → $\boldsymbol{\sigma_{Jitter} = \dfrac{t_{rise}}{Signal/Noise} \sim 25}$ **ps**



From: 1704.08666

- **Timewalk effect:**
  Time-Of-Arrival (TOA) depends on signal amplitude
  → $\boldsymbol{\sigma_{Landau} = \left.\dfrac{V_{th}}{Signal/t_{rise}}\right|_{RMS}}$
  → Can be corrected based on ToT

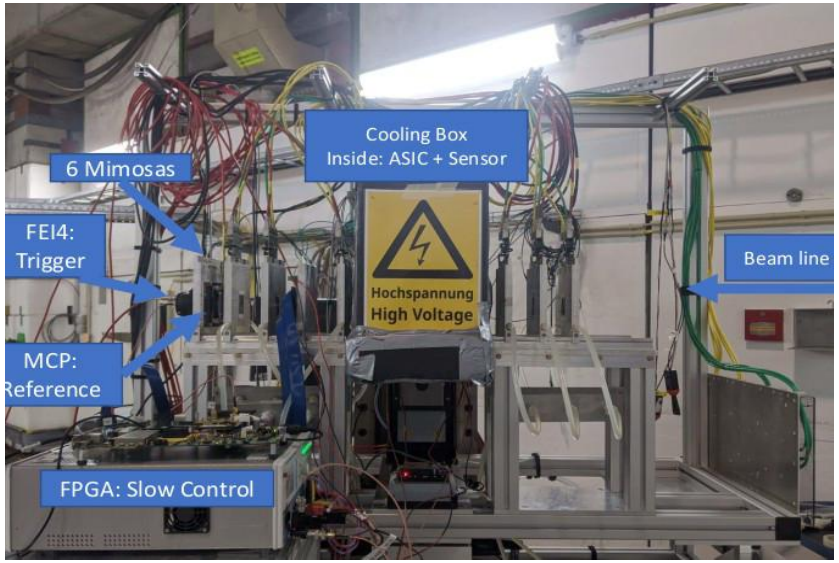
- **TDC:**
  From TDC binning / non-linearity
  → $\boldsymbol{\sigma_{TDC} \geq LSB/\sqrt{12} = 6}$ **ps**

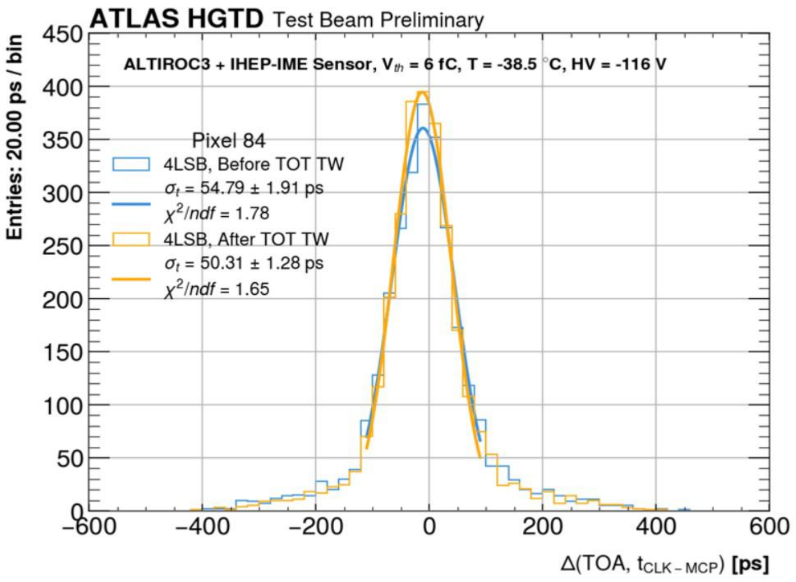
- **Clock:**
  Jitter of the 40 MHz clock
  → $\boldsymbol{\sigma_{Clock} < 10}$ **ps**

ALTIROC tests

- Tracking and timing setup
- Micro-channel plate (MCP) for timing reference
- Δt from ToA and MCP timing
- Pre-production LGAD sensors and **ALTIROC3** ASIC used

2024 beam tests at DESY and CERN





- Δt distribution before (blue) and after (orange) Time-Walk correction
- Operated at cold temperature (un-irradiated)

- Obtain **≈ 50 ps** in average
  - *Carbonated LGADs!*
- Improvements implemented in ALTIROC-A
  - Final design

The HGTD Modules

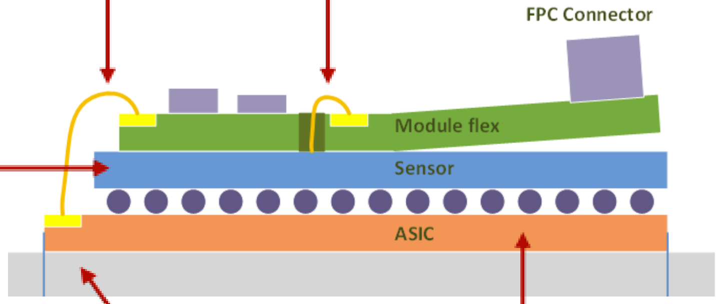
An **HGTD module** consists of:

- Two **sensors** 15x15 pads (2 cm × 2 cm) each
- Two **ALTIROC ASICs** (2 cm × 2 cm) each
- A **module flex**
- A **flex tail**

Wire bonds

HV wire to sensor back-side

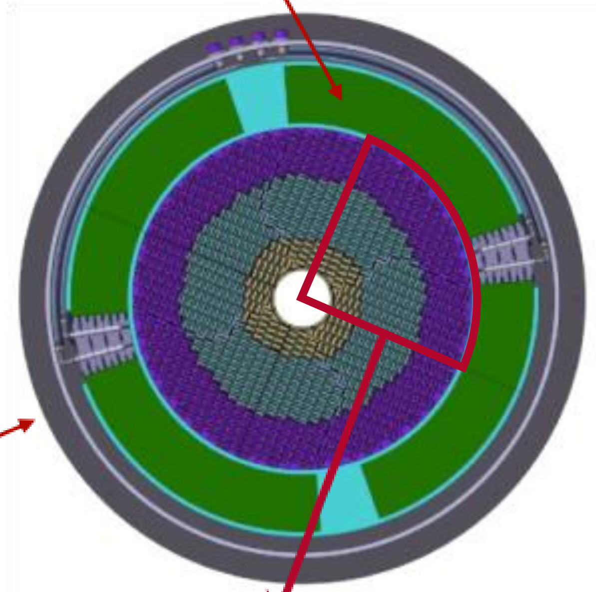
LGAD sensor



Cooling plate

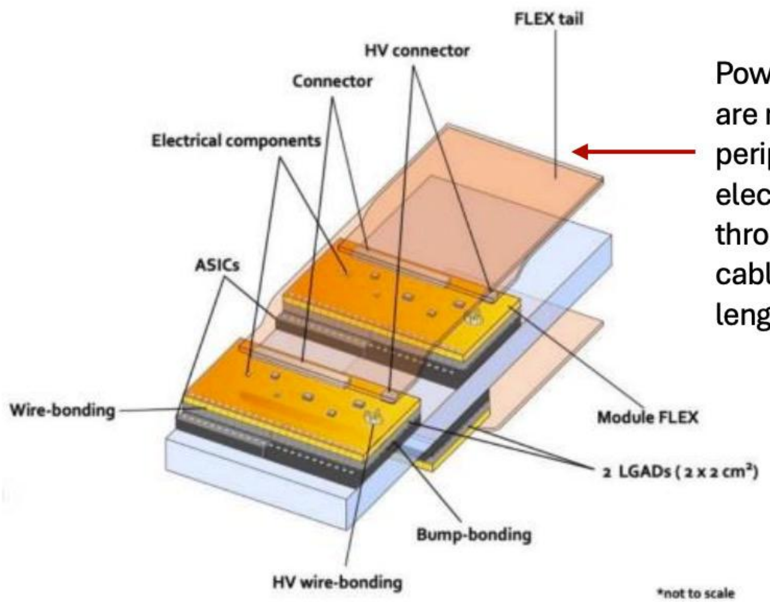
ASIC bump-bonded to sensor

Peripheral Electronics Board (PEB)

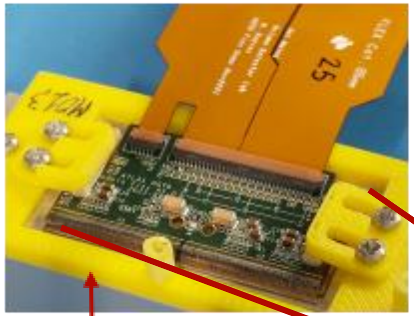


An HGTD disk

Disk quadrant of the HGTD active region (24DUs)

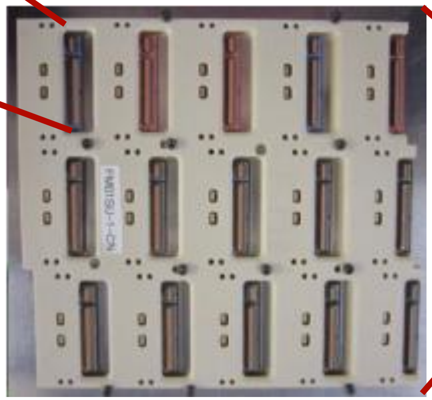


Power and signal are routed to the peripheral electronics through flexible cables of different lengths (flex tail)



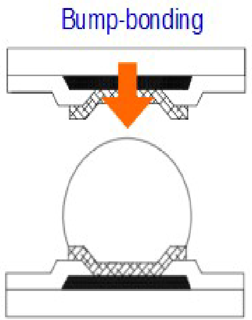
Module

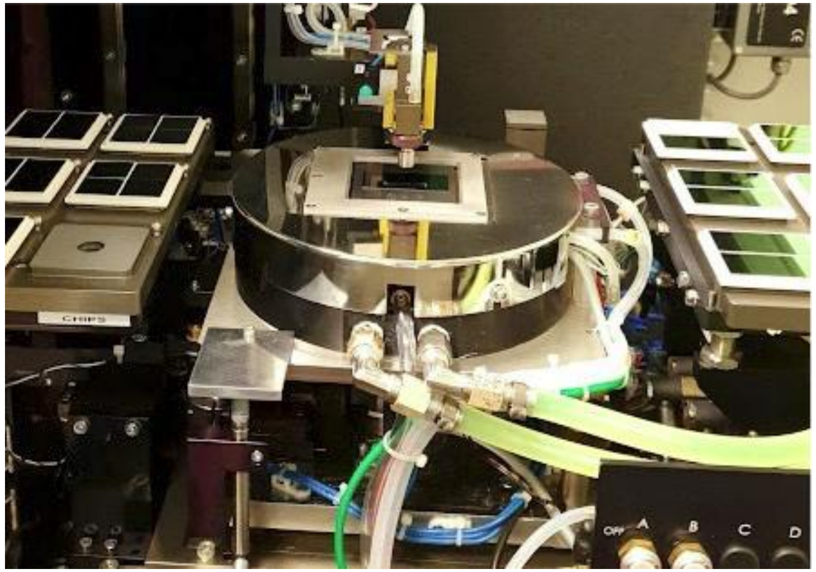
Detector Unit (DU)



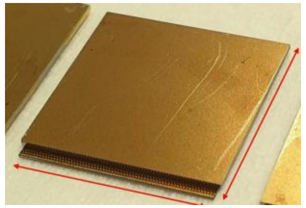
https://indico.cern.ch/event/1469148/contributions/6460347/

HGTD module assembly

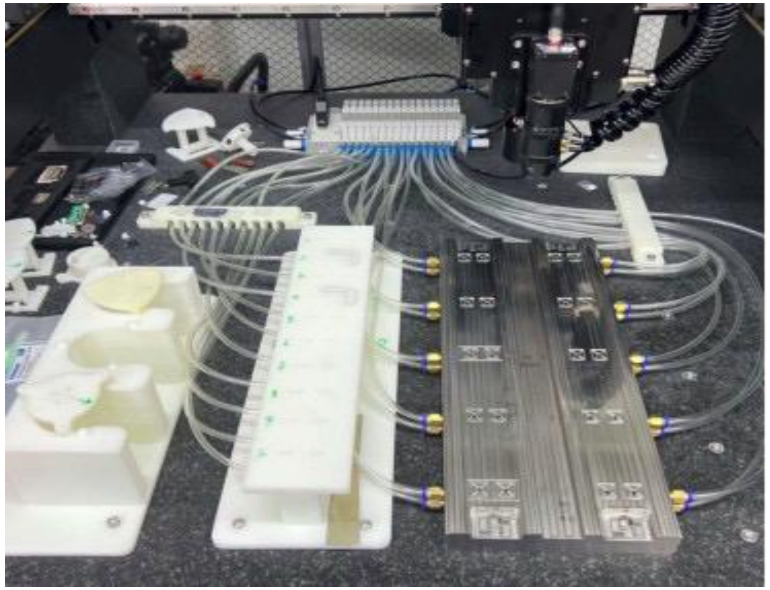




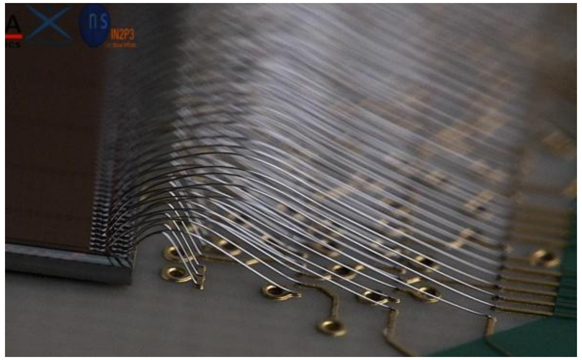
Bump bonding with 100 μm balls



Assembled hybrid undergo X-ray control



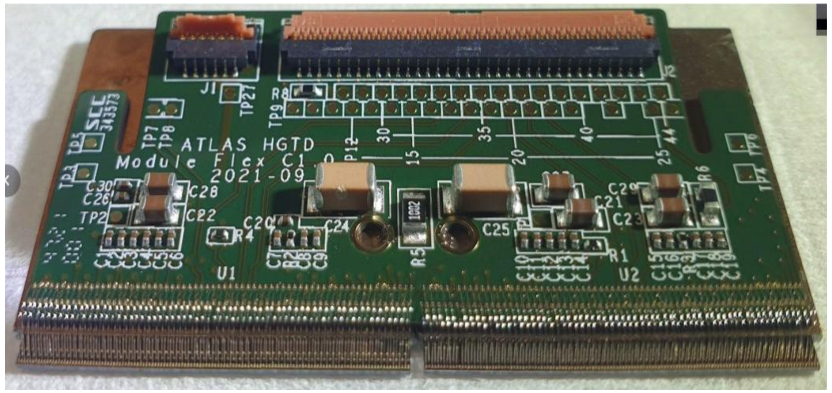
Module assembly:
gluing 2 hybrids to module PCB



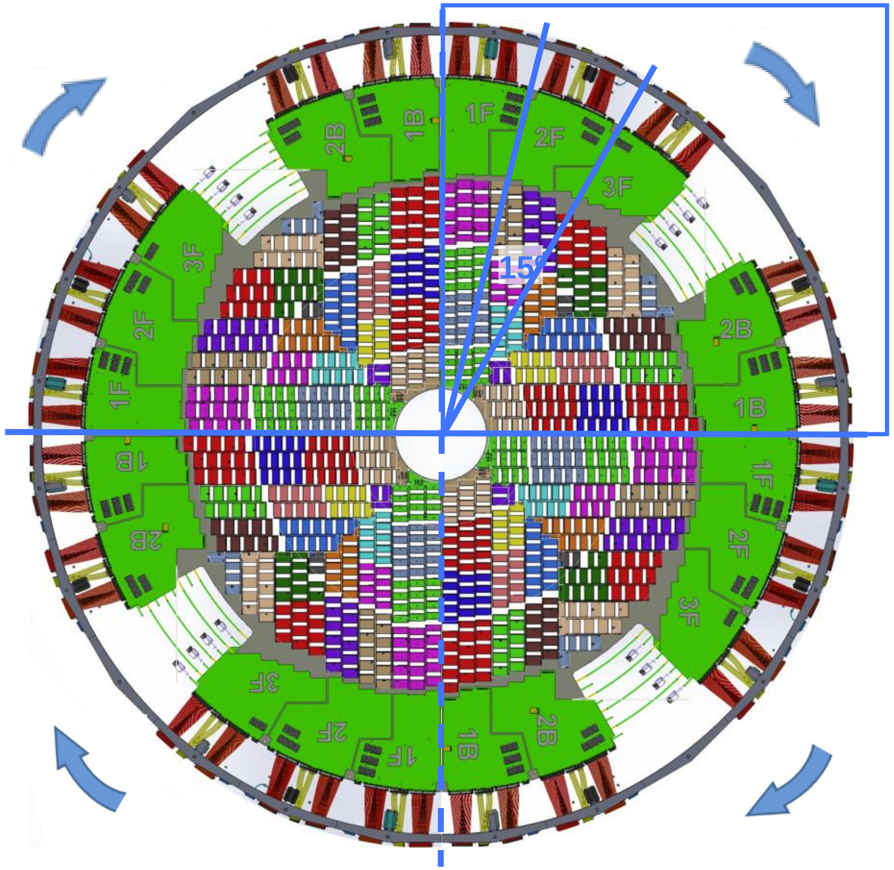
Wire bonding

Module test

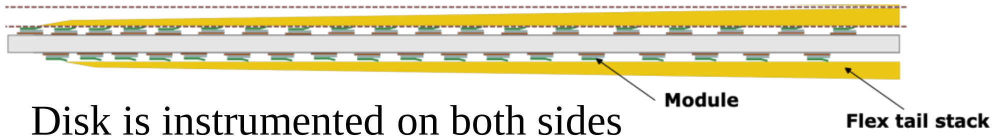
Assembled module



Instrumented disks layout



Front side if instrumented disk
(flex tails are not shown)



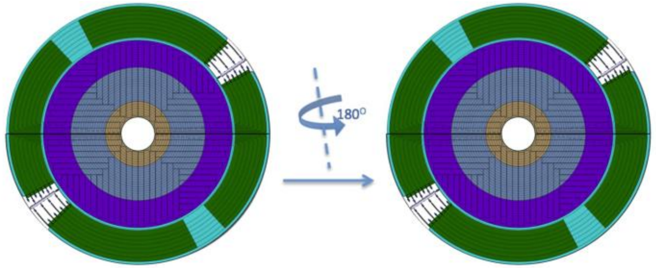
Disk is instrumented on both sides

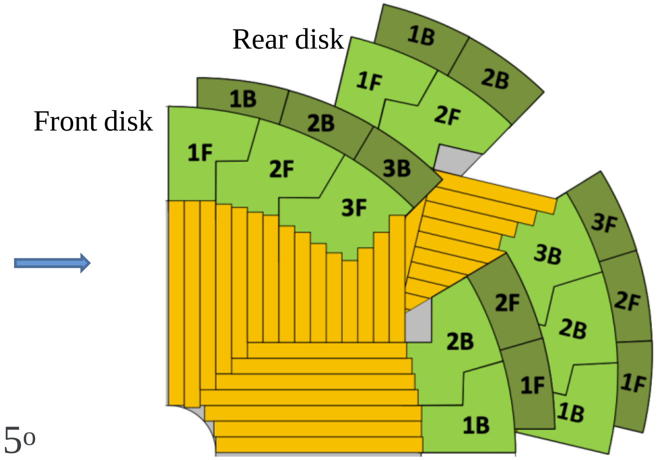
Design of HGTD detector is optimized to maximize number of identical components:

- all disks are instrumented equally, composed of 2 identical half-disks
- all quadrants of disk are identical
- only 6 different types of PEBs are used
- positions connectors on PEB and on 15° section of outer ring are the same for each PEB
- all pigtails and fanouts of the same type are identical
- number of identical flex tails is maximized.

➢ **It is sufficient to consider only one quadrant of the instrumented disk**

➢ **It is sufficient to define the arrangement and lengths of PEB services Only in one of the 15° sections.**

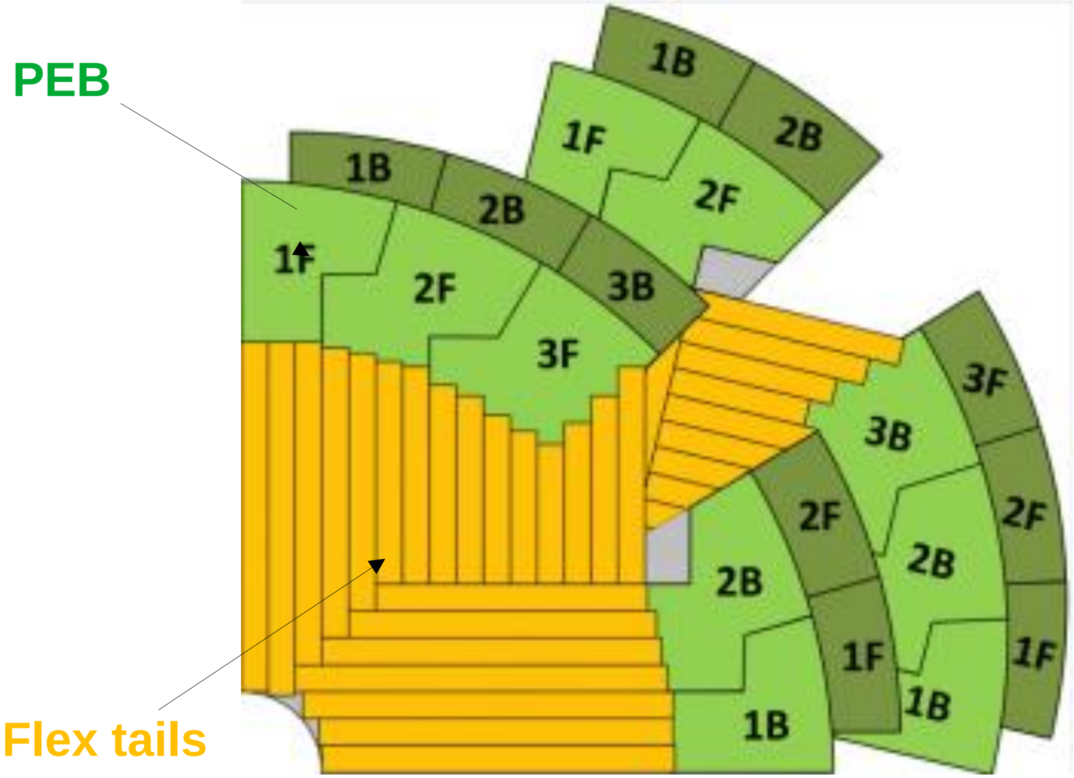




Rear disc is turned face-back to create a 15° angle between rows of modules on the discs

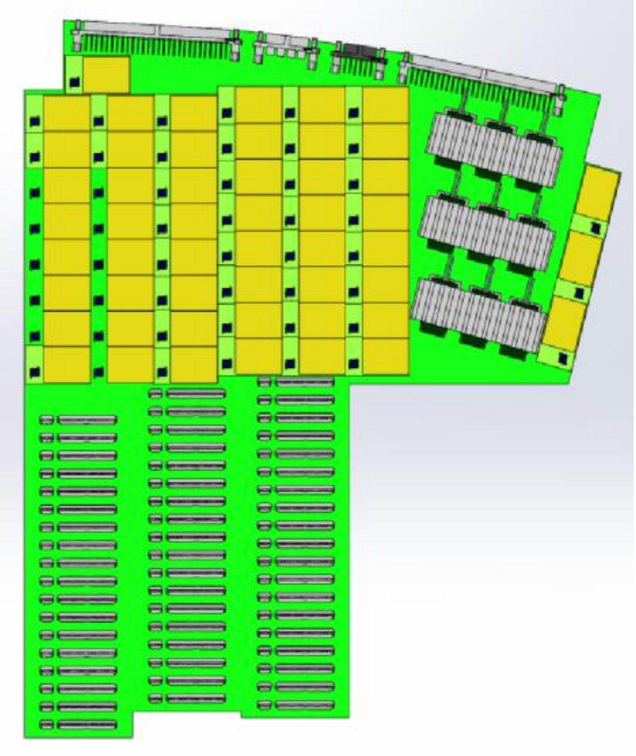
Peripheral Electronic Board (PEB)

Front-end modules connected to the PEB through Flex Tails

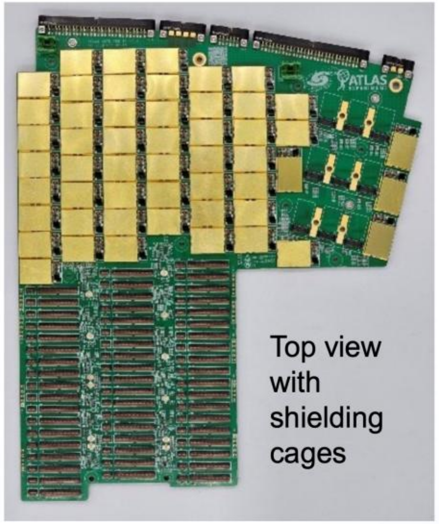


- Six types of PEB to be designed (front and back side)
  (boards 1F, 2F, 1B and 2B can be used on both sides)

1F	2F	3F	3B	2B	1B	Total
32	32	16	16	32	32	160



1st prototype PEB (1F)

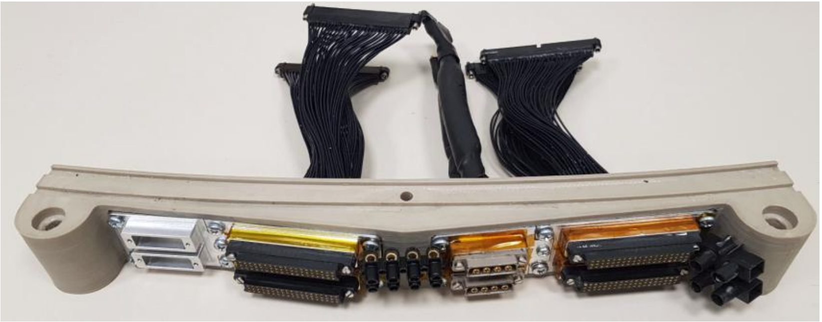


- Very complex PCB design
  (22 layers)

Peripheral board	Modules	lpGBT	bPOL12v	MUX	VTRx+
1F	55	9+3	52	9	9

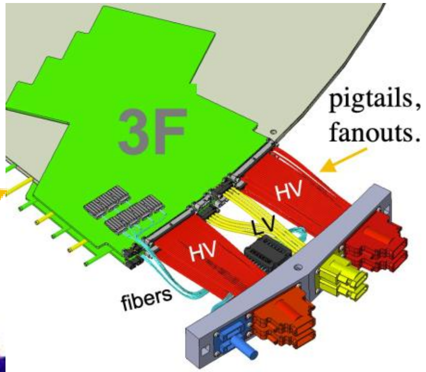
HGTD vessel

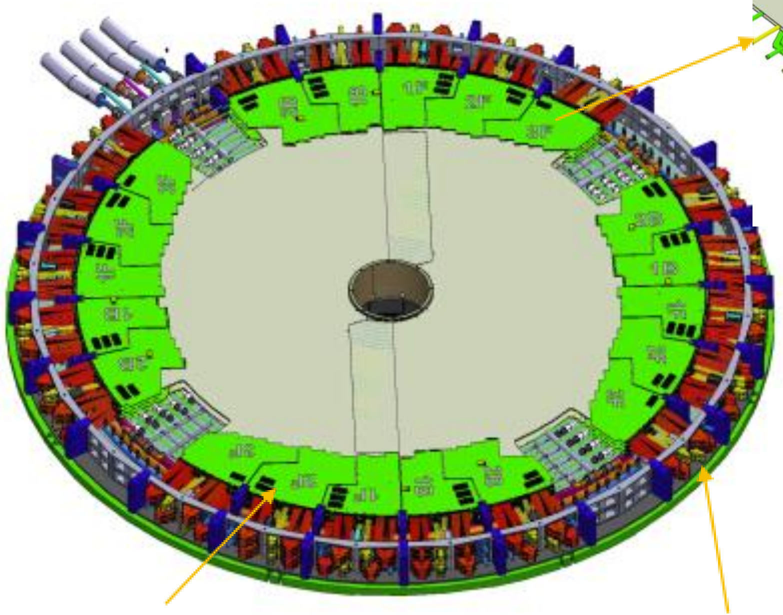
- ~300 cables and 40 optical cables connected to each vessel at outer ring
- 281 pigtails + 80 optical fanouts per vessel interconnect PEBs with cables
- HV, LV, NTC pigtails all are identical, fanouts are the same length
- Vessel is made as a Faraday cage



All sections of outer ring will be pre-assembled with services. First prototype shown in picture.

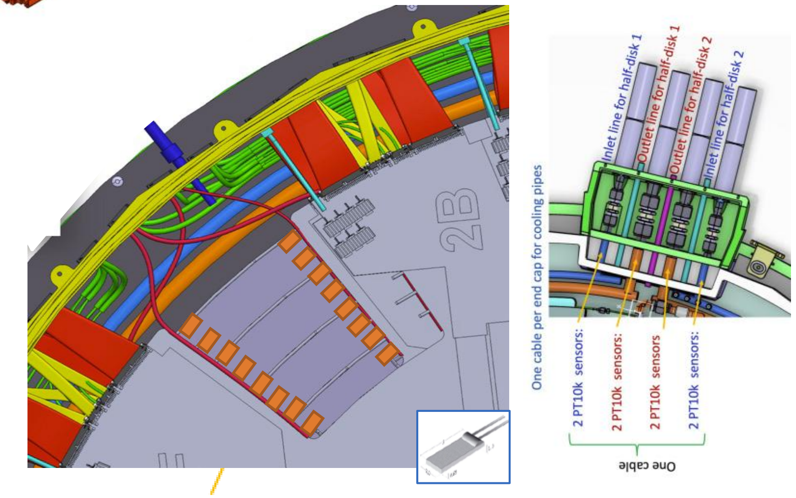
Prototype of assembles outer ring section



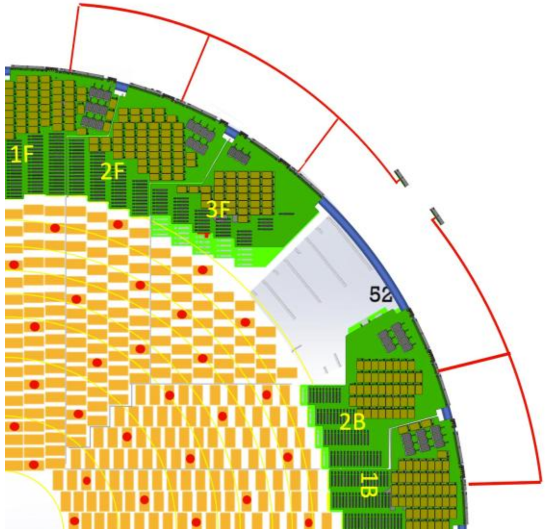


Peripheral electronics

All cables and fibers connected to outer ring.



PT10k on cooling loops of half-disk

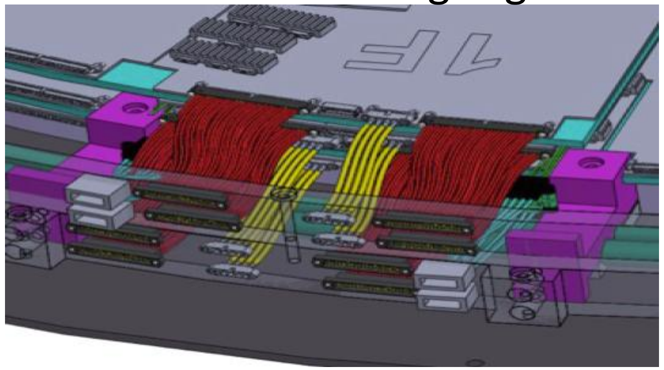


NTC sensors on modules

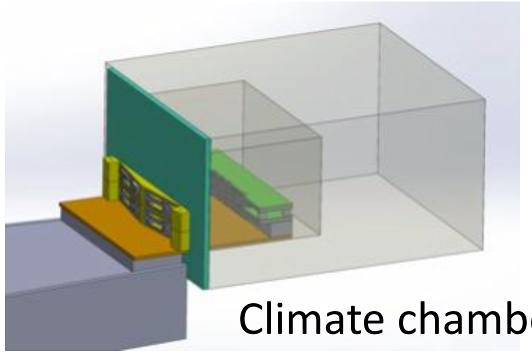
Contributions of Wits/ICPP to the HGTD

- In June 2025, Wits/ICPP was voted to join the HGTD project
- Our members have been contributing already to the project
  - Thabo Lepotha (see next talk): works on HGTD demonstrator and testbeam
  - Katlego Machethe (Ithemba/Wits) is working on DAQ system and PEB-FELIX interface
- Main contribution to the HGTD heater system
  - Avoid condensation effect on electronics interface between the inside vessel (-30^{o} C) and the ATLAS Cavern
  - On going tests with mock-up of an outer ring segment

HGTD outer ring segment



Mock-up segment



Climate chamber, ~30^{o}C

HGTD Heater tests

Al plate for optic connectors 27°C

Heater power on HV connector 6.7 W
Temperature of heater 31 °C
Temperature on contacts 21 °C

Heater power on LV connector 3.1 W
Temperature of heater 29 °C
Temperature on contacts 18-19 °C

Heater power on HV connector 6.8 W
Temperature of heater 29 °C
Temperature on contacts 18-20 °C

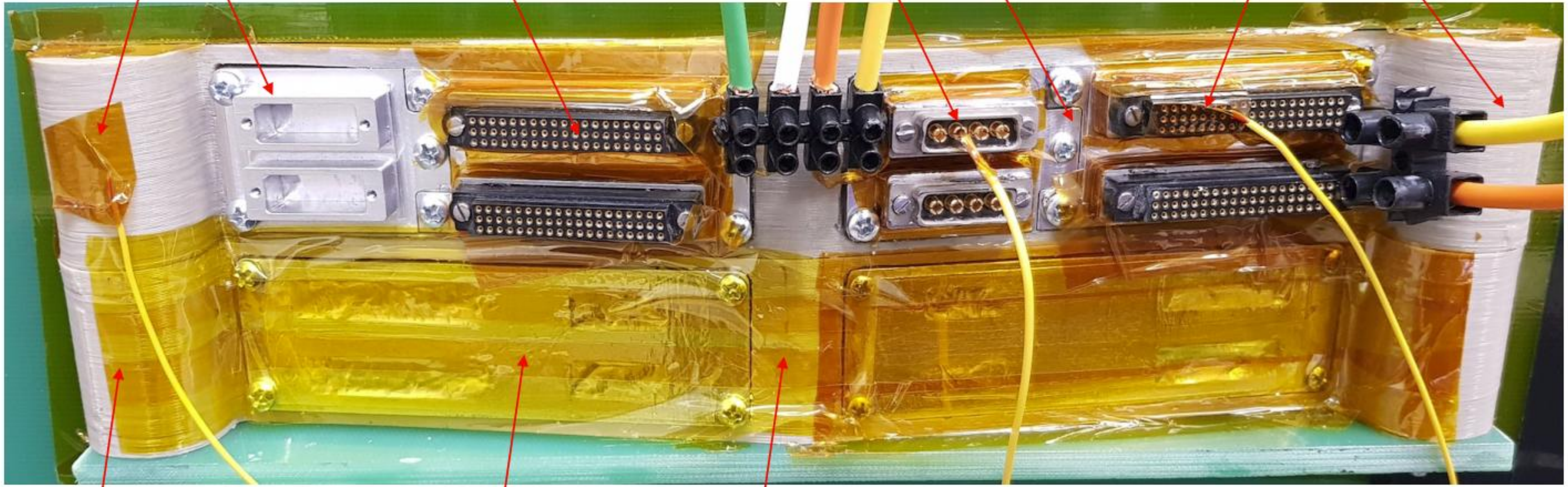
Top section of OR with heaters

Peek on left side 20°C

PEEk in middle 21°C

Al plate in middle 25°C

Peek on right side 21°C

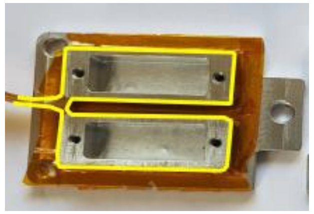


Bottom section of OR without heaters

Peek on side 19°C

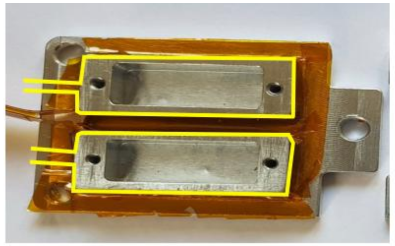
Al plate 14°C

PEEk in middle 16°C

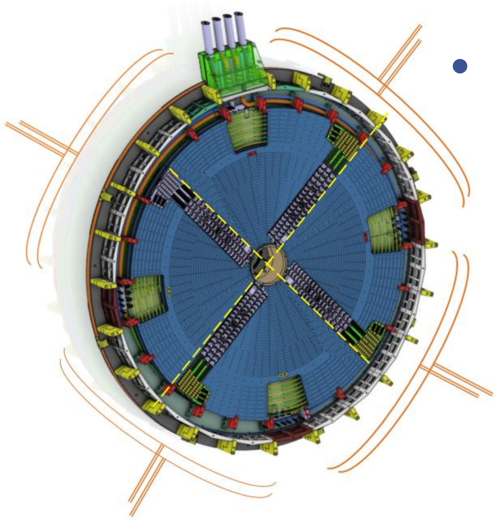


Heaters: 80/20 NiCr resistance flat wire over perimeter connectors

HGTD requirements

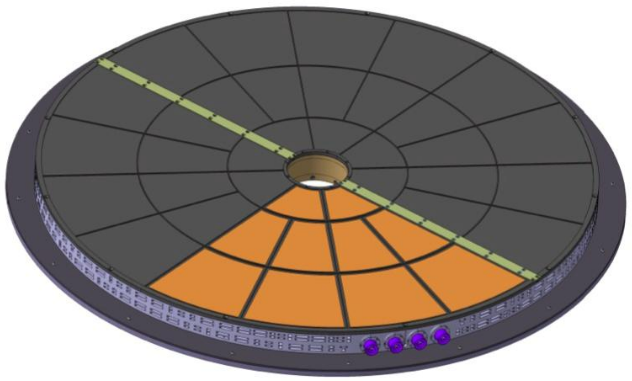


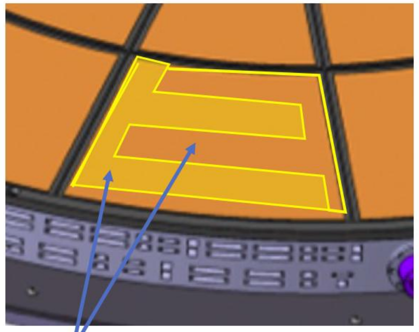
- Heater on vessel outer ring. Redundancy a crucial issue



- Example of PS heaters for the full vessel
  - Heaters on HV connectors can be connected in series: 2x2 connectors x 5 OR sections = 20 HV connectors, 8 series per vessel
  - Such a grouping requires 16 heater PS channels for 2 end caps, with power of about 150 W / channel.

Heater type	50W heater	150W heter
On LV connectors	8	
On HV connectors		16
On DCS connectors	12	
On humidity sensor	1	
Total heaters	22	16





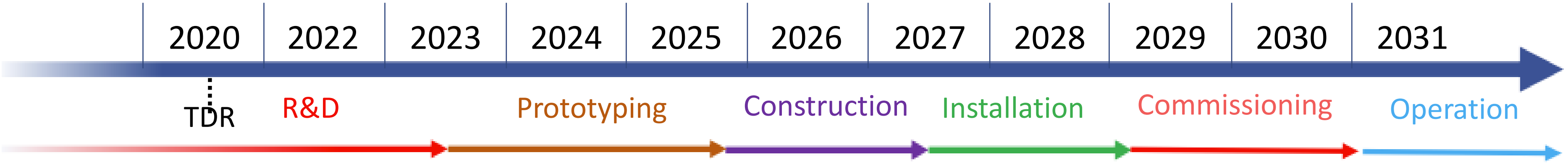
2 heaters connected in parallel to the same PS channel. If one fails, another is able to heat this zone.

- **Several PS channels are required for heaters on vessel front cover,**
- **Heaters should be interconnected in series and redundancy also must be implemented**

Conclusions

- HGTD will provide precision timing information for charged particles in the forward region of ATLAS along with luminosity measurements during full life of HL-LHC
- LGAD sensors and front-end ASICs ALTIROC meet requirements up to fluence of 2.5 x 10^{15} n_{eq}/cm^2
- HGTD design is progressing well, detector subsystems nearing Final Design and Production
- The workload is evolving towards testing of mechanics, services, cooling, back-end electronics, preparing for detector assembly. Test beam activity are ongoing.
- Tests of the HGTD demonstrator built around the 1F PEB are in progress.
- Slowly moving towards mass production and construction of HGTD

- Involvement oof Wits/ICPP presents am opportunity to develop local expertise in Silicon detector system
- Heater system design, optimisation



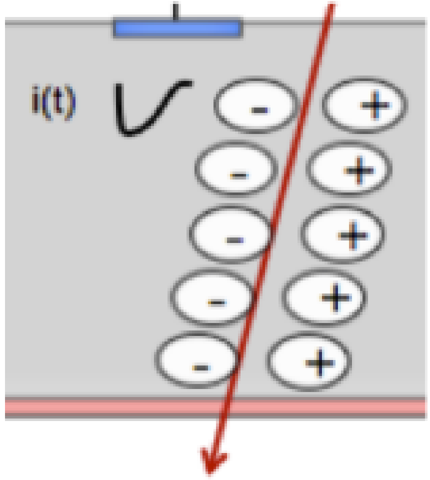
Additional material

Low Gain Avalance Diode (LGAD) sensors

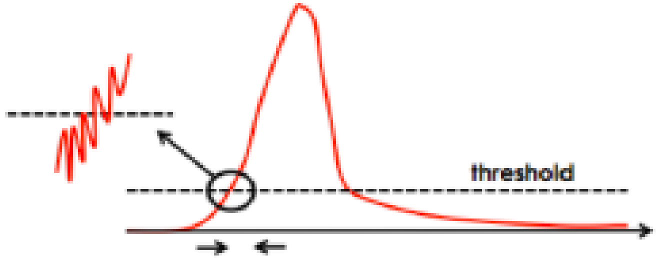
overview of contributions to the time resolution:

$$\sigma^2_{hit} = \sigma^2_{Landau} + \sigma^2_{jitter} + \sigma^2_{time-walk} + \sigma^2_{TDC} + \sigma^2_{clock}$$

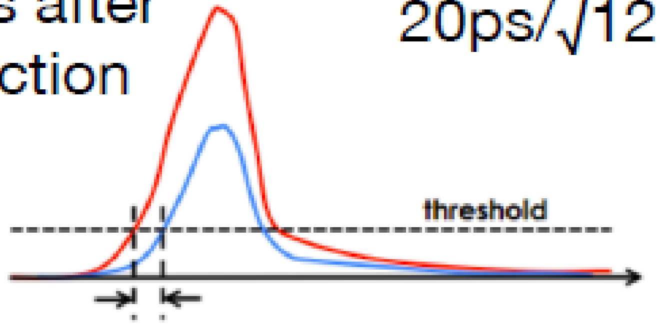
~25 ps
(thin sensor)



<25 ps at
large gain



<10 ps after
correction

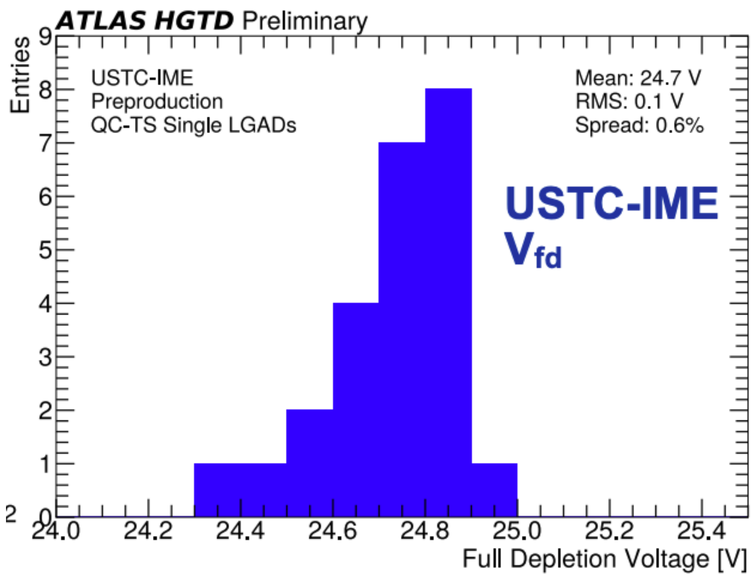


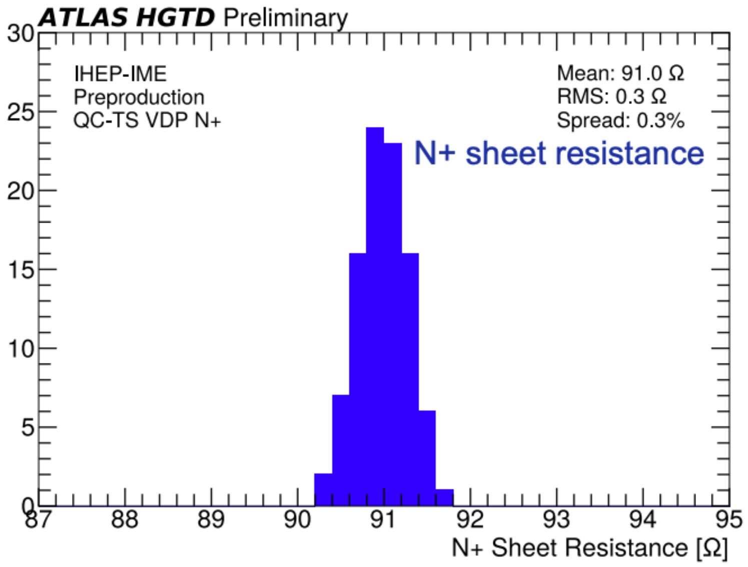
bin width,
20ps/√12

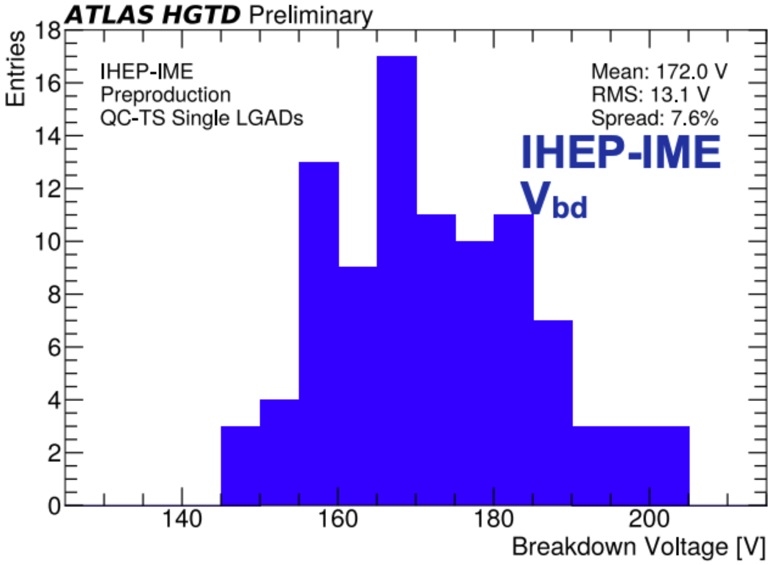
from clock
distribution, <10ps

QC-TS pre-production results

- Measurements on ~10 **QC-TS** per wafer for both vendors
- Results consistent within the specifications / expectations
  - **Break-down voltage**: V_{bd} spread 5.6% - 7.6% (spec: <8%)
  - **Full-depletion voltage**: V_{fd}<30 V (spec: <70 V), spread <10%
    → resistivity >1 kOhm*cm
  - **Gain-layer depletion voltage**: 24 V < V_{gl} < 55 V
  - **Detector capacitance**:
    Cdet ~ 4.2-4.4 pF (spec: <4.5 pF)
  - **Oxide thickness**: $\sigma(t_{ox})/ t_{ox} < 3\%$
  - **n+ sheet resistance**: <0.3% spread
  - **Inter-pad gap**: ≲100 μm







https://twiki.cern.ch/twiki/bin/view/AtlasPublic/HGTDPublicPlots
https://indico.cern.ch/event/1386009/contributions/6279120

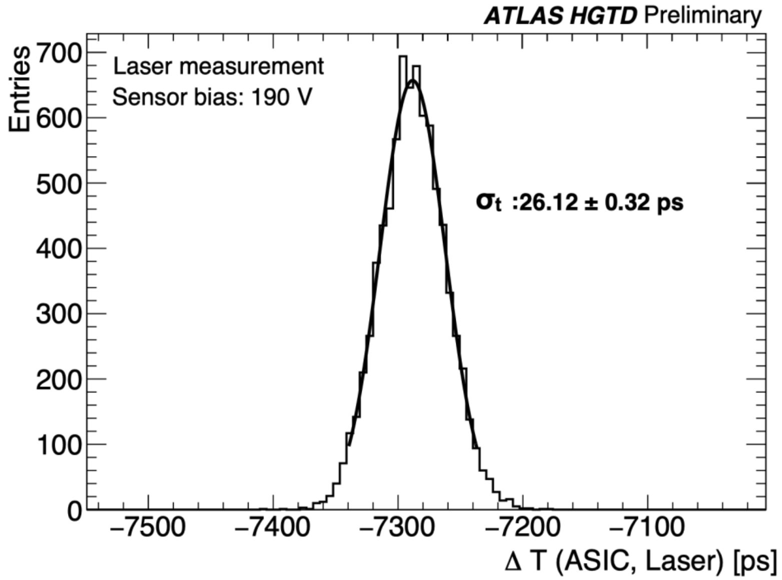
ATLAS EXPERIMENT

Jitter Measurements

- **Infrared laser** (1064 nm, sub-mm focus) used to determine jitter
- **Uniform deposition** of constant energy in the sensor

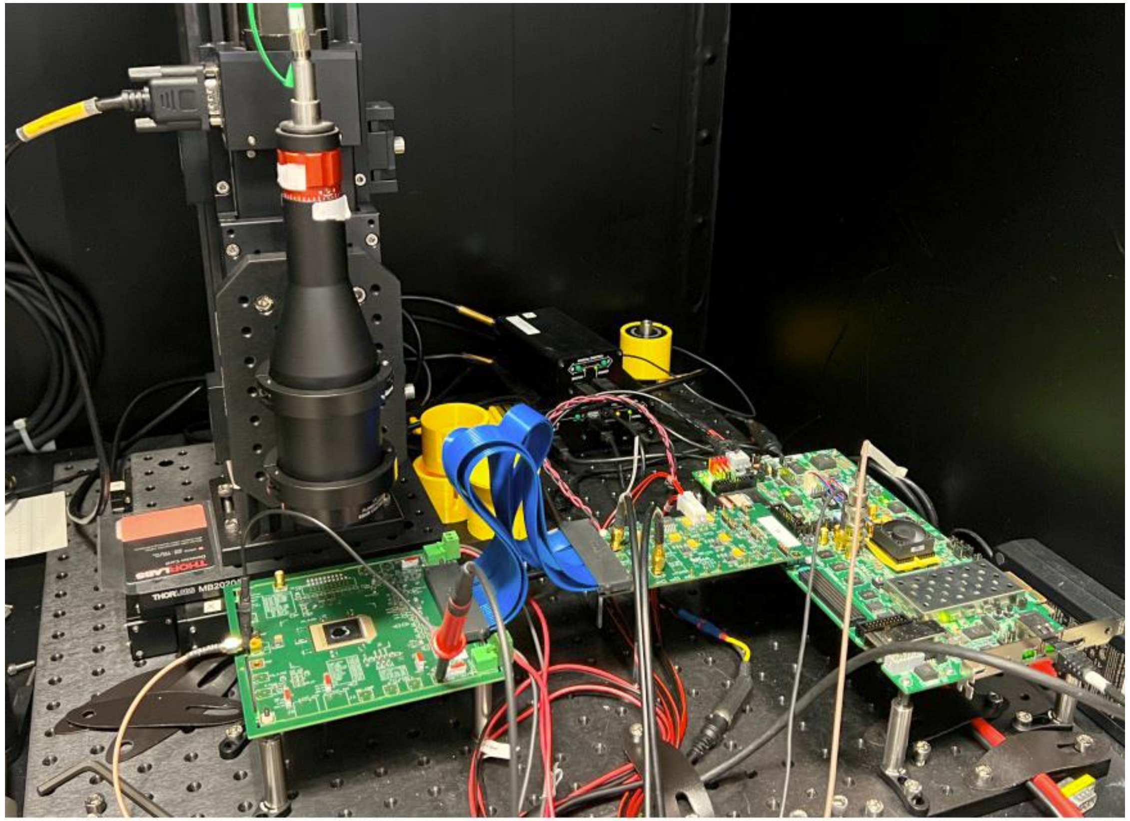
  → Landau and Timewalk contributions negligible
- Time reference: precise signal (3 ps jitter) from laser driver
- Jitter measured to be **~25 ps**

  → Consistent with ASIC test-bench measurements



sensor | read-out electronics

$$\sigma^2_{\text{total}} = \sigma^2_{\text{Landau}} + \sigma^2_{\text{Timewalk}} + \sigma^2_{\text{Jitter}} + \sigma^2_{\text{TDC}} + \sigma^2_{\text{Clock}}$$



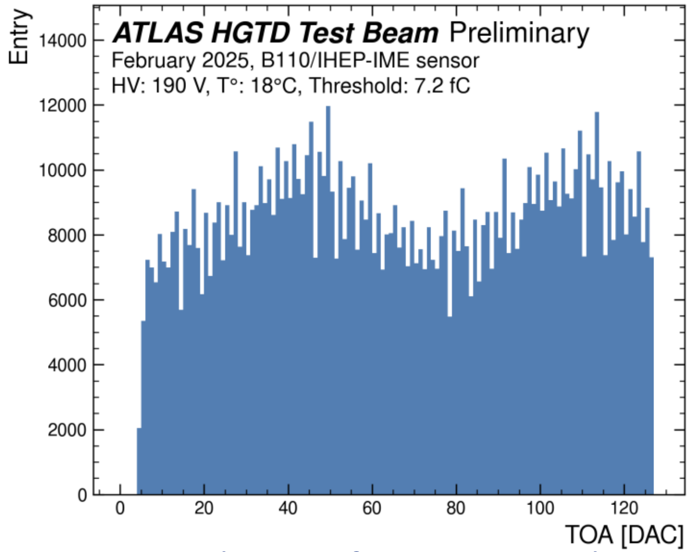
TDC bin corrections

- **ToA** measurement based on Time-to-Digital Converter (**TDC**)
- Quantization error given by TDC quantization step size (Least Significant Bit = LSB)
- Nominal LSB value: **20 ps**
- Observed LSB shows variations over the 128 ToA bins from Differential Non Linearity (**DNL**)
- LSB values depend also on temperature and stability of power supplies

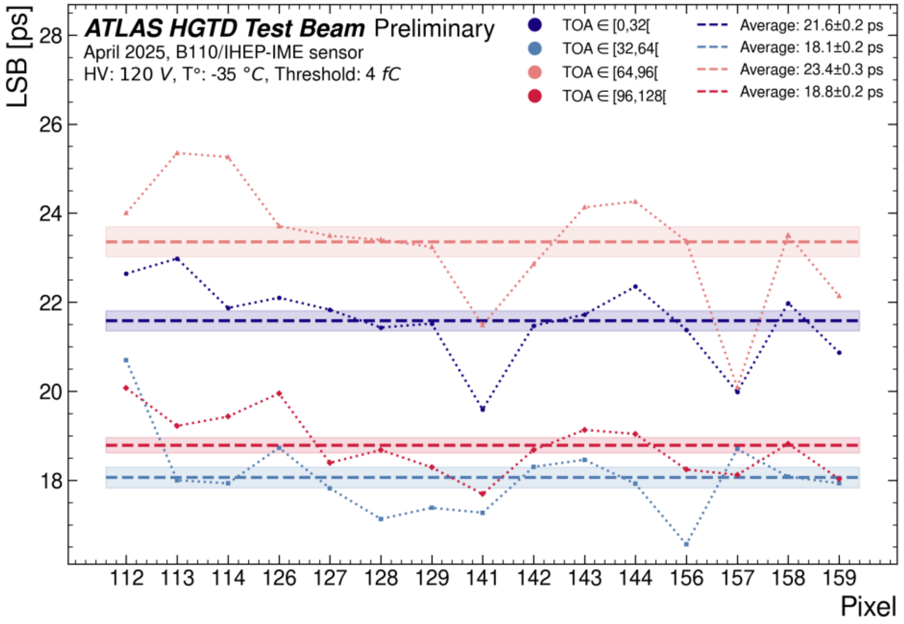
→ Several methods developed for **in-situ calibration** of LSBs per-pixel:

- Internal charge injection in ASIC
- Data-driven calibration from high-statistics test-beam data sets:
  - Either one **global LSB** value per pixel
  - Or one LSB value per group of **32 ToAs** → gives best results

ToA distribution in test beam



Distribution of 4 LSBs per pixel



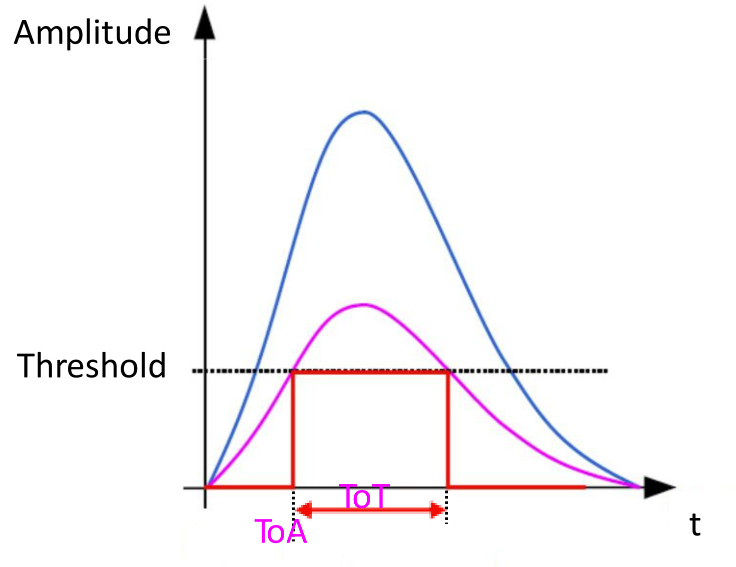
https://twiki.cern.ch/twiki/bin/view/AtlasPublic/HGTDPublicPlots

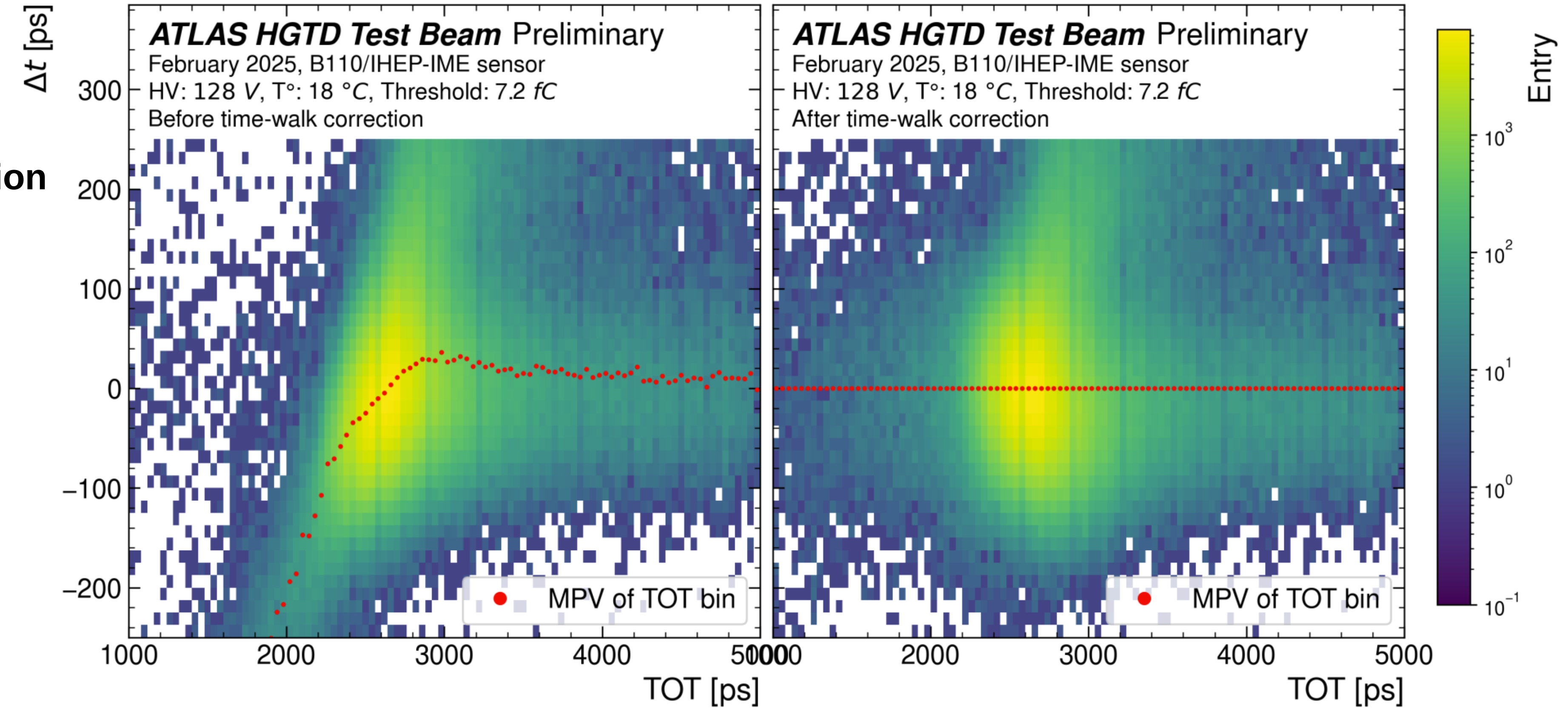
Timewalk Correction

- **Timewalk** effect: ToA depends on signal amplitude (at constant threshold)

→ **ToA** and **ToT** are **correlated**

- Use correlation to obtain **correction**
- Time-walk effect largely reduced after correction





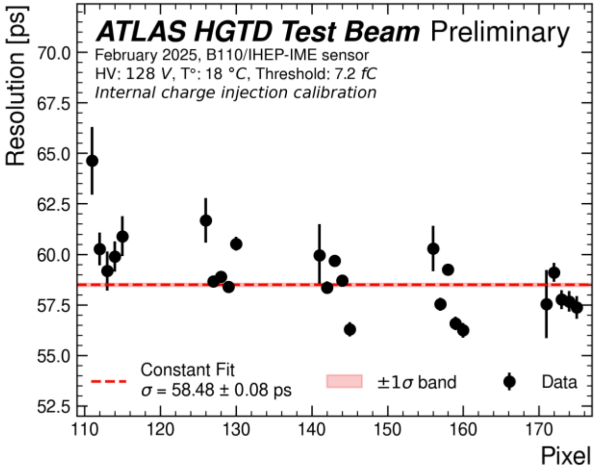
https://twiki.cern.ch/twiki/bin/view/AtlasPublic/HGTDPublicPlots

https://twiki.cern.ch/twiki/bin/view/AtlasPublic/HGTDPublicPlots

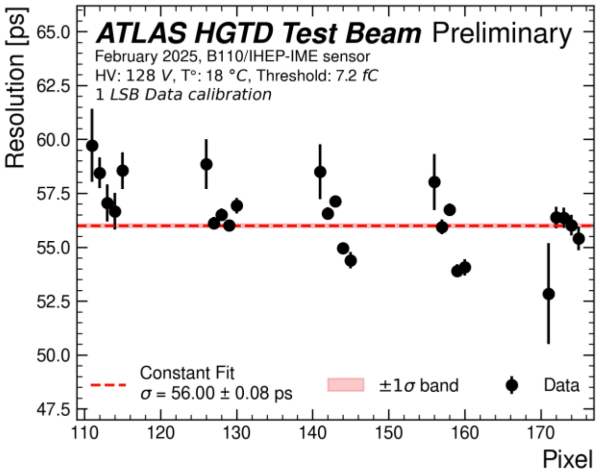
Hybrid test-beam measurements – ToA calibration

- **Time resolution** is extracted from residuals between ToA measurement and MCP-PMT time reference (tracking not used → sample contains events from the pixel borders)
- ToA values are calibrated:
  - **LSB** of TDC (from charge injection / data-driven)
  - **Time-walk** effects (data-driven)
- Time resolution improves significantly when using data-driven methods and accounting for DNL of TDC

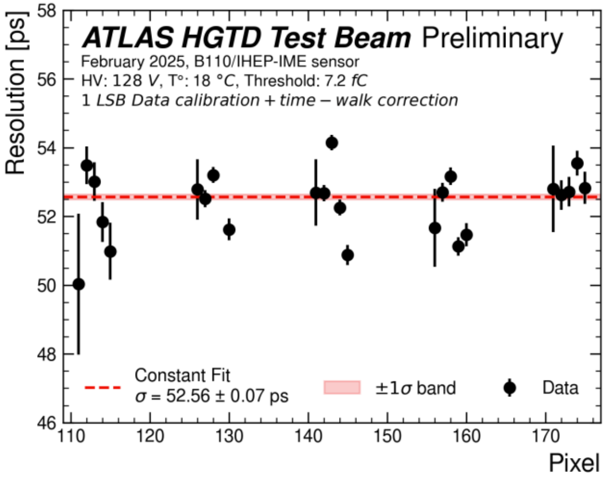
Constant LSB (charge injection), no TWC



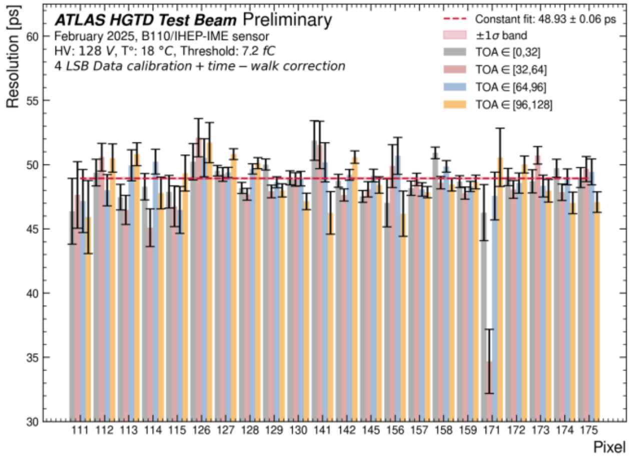
Constant LSB from TB data, no TWC



Constant LSB from TB data, with TWC



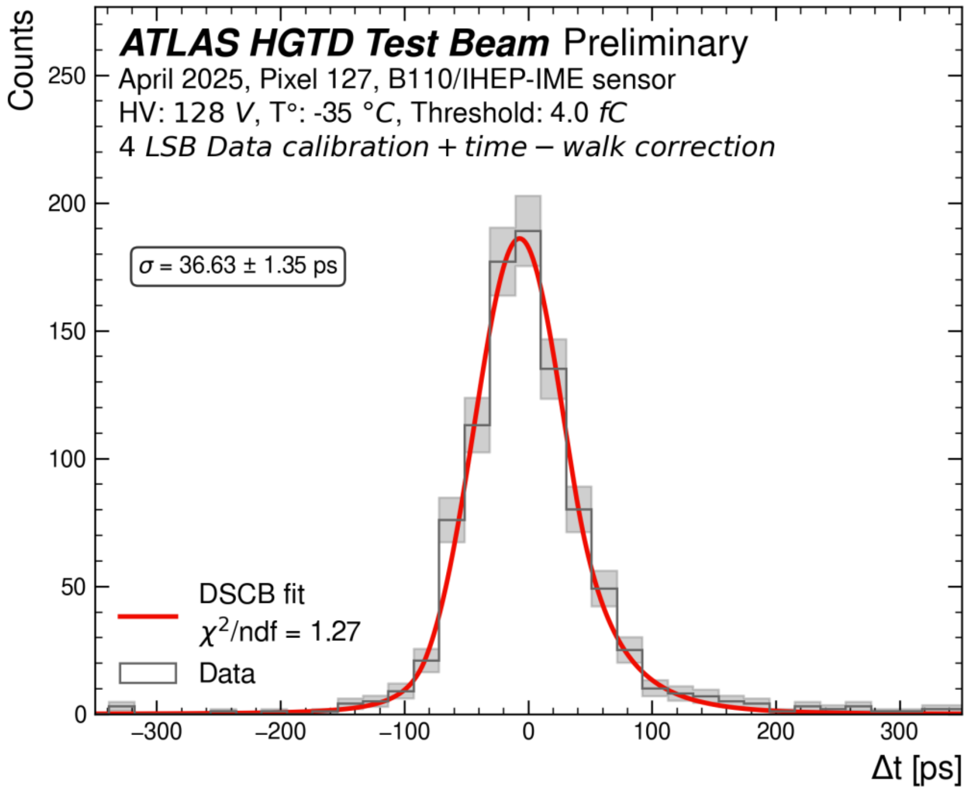
4 LSB from TB data, with TWC

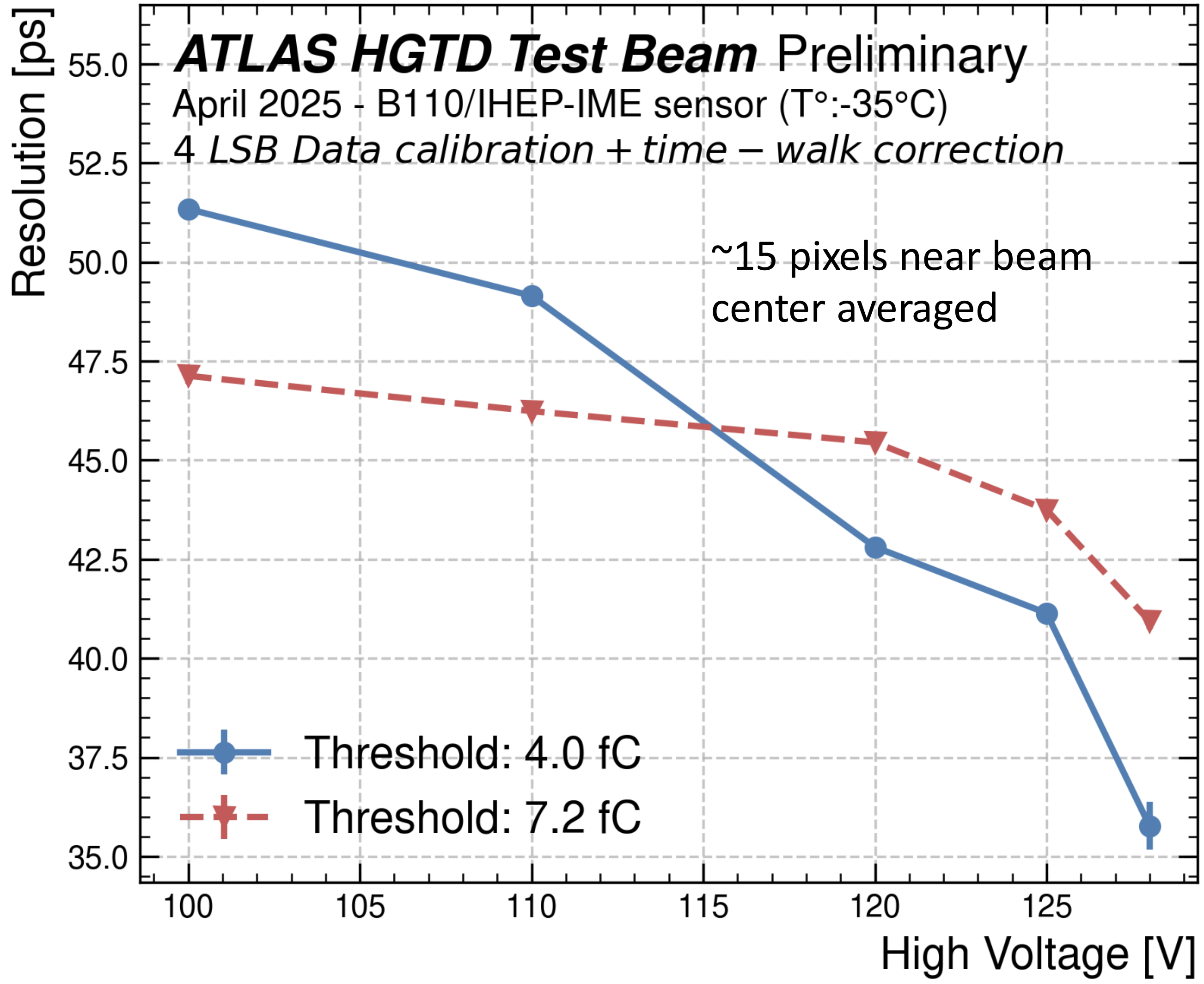


Hybrid test-beam performance

https://twiki.cern.ch/twiki/bin/view/AtlasPublic/HGTDPublicPlots

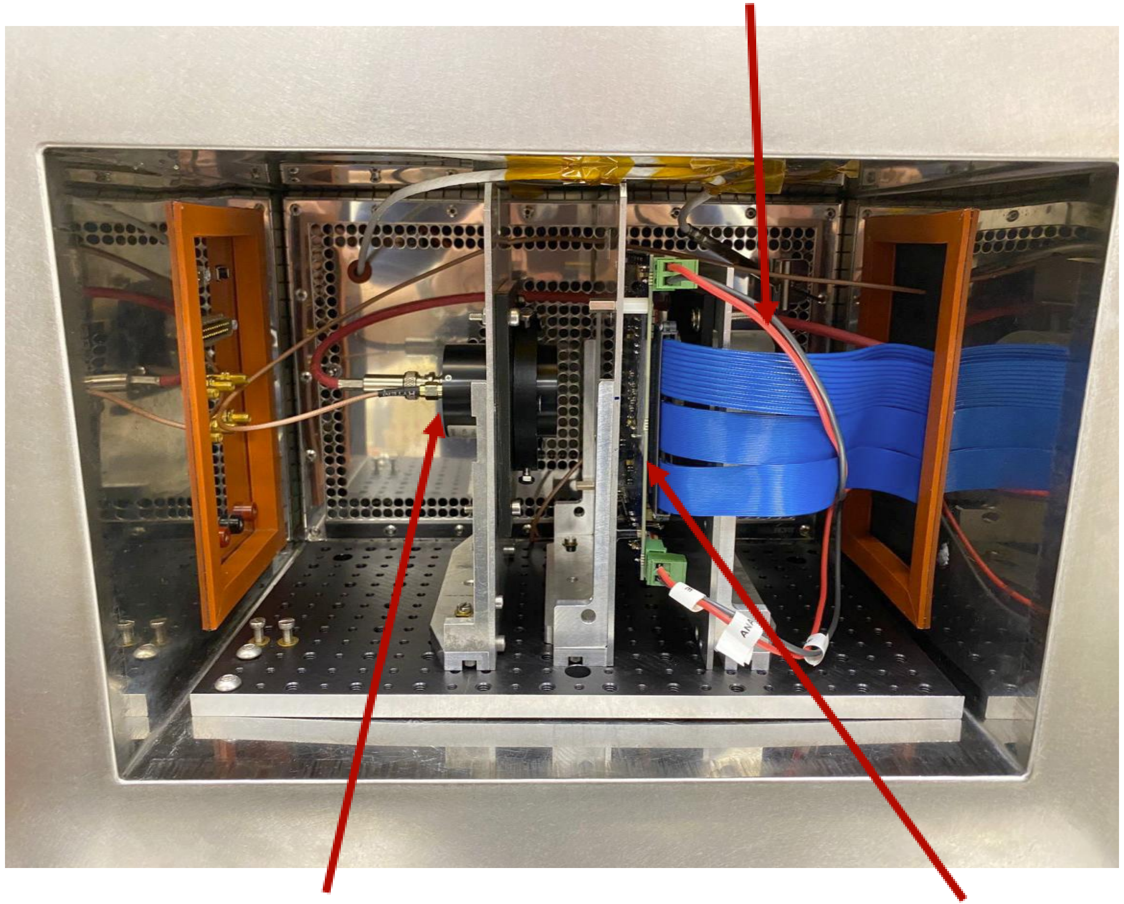
Performance measurements in **optimal conditions**:
Low temp. (-35º), high bias voltage (>120 V), low thr. (4 fC)
→ Timing precision in core of distribution down to **~40 ps**





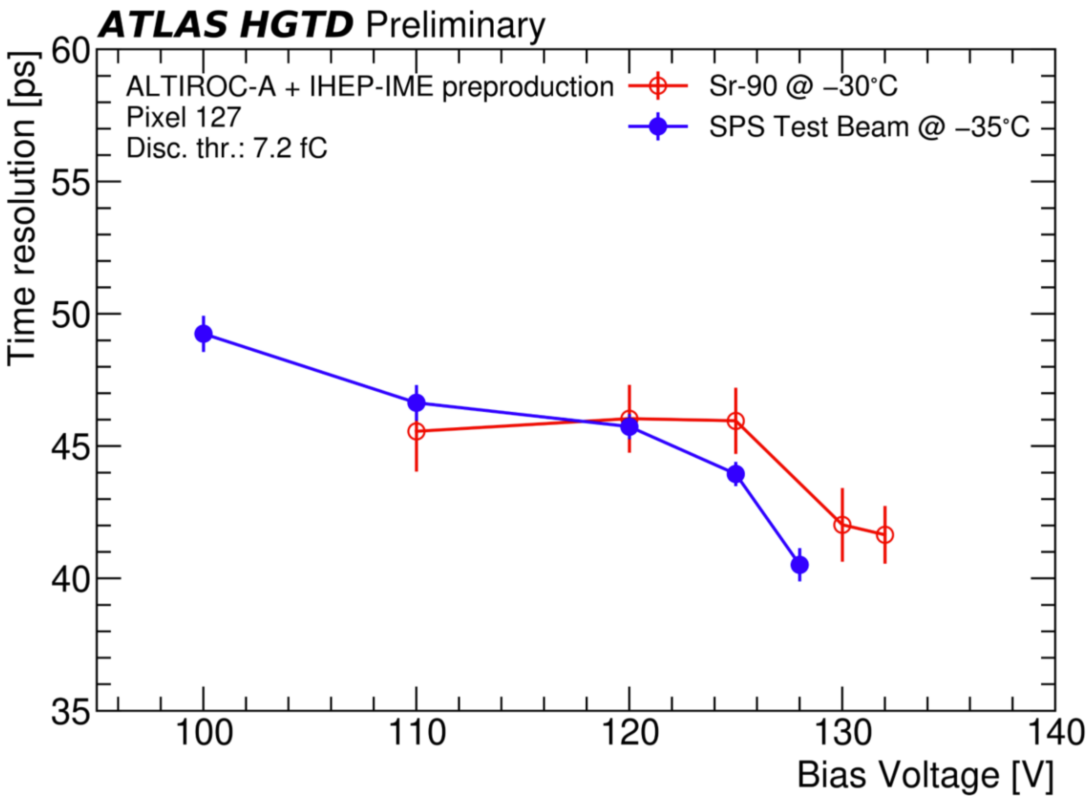
Hybrid timing measurements with β-source

Sr-90 source (~ 30MBq)



MCP-PMT (time reference)

ALTIROC-A + LGAD test board

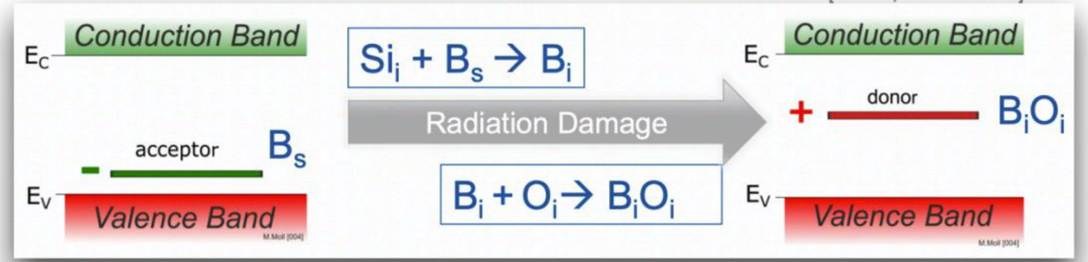


- Least Significant Bit (**LSB**) calibrated to 20 ps (charge inj.)
- **Time-walk** correction applied for DUT; CFD for MCP-PMT
- Time **resolution**: Std. dev. of Gaussian fit of TOA_{DUT} – TOA_{M}
  - **~ 45 ps** achieved for 7 fC threshold, consistent with test-beam results
  - **Uniform** behavior for all pixels

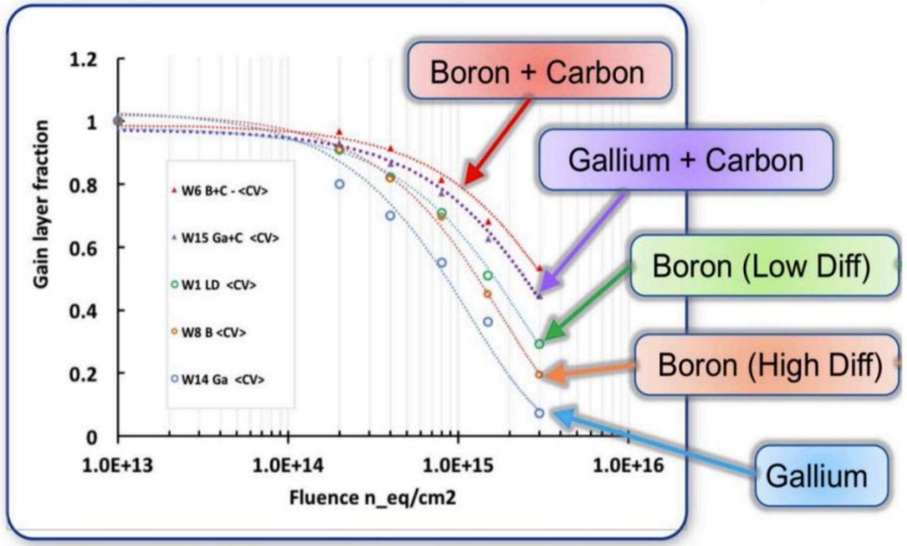
Carbon implantation

- The reduction of effective doping in the gain layer is caused by the "acceptor removal" process →LGAD gain reduction after non-ionizing radiation damage.

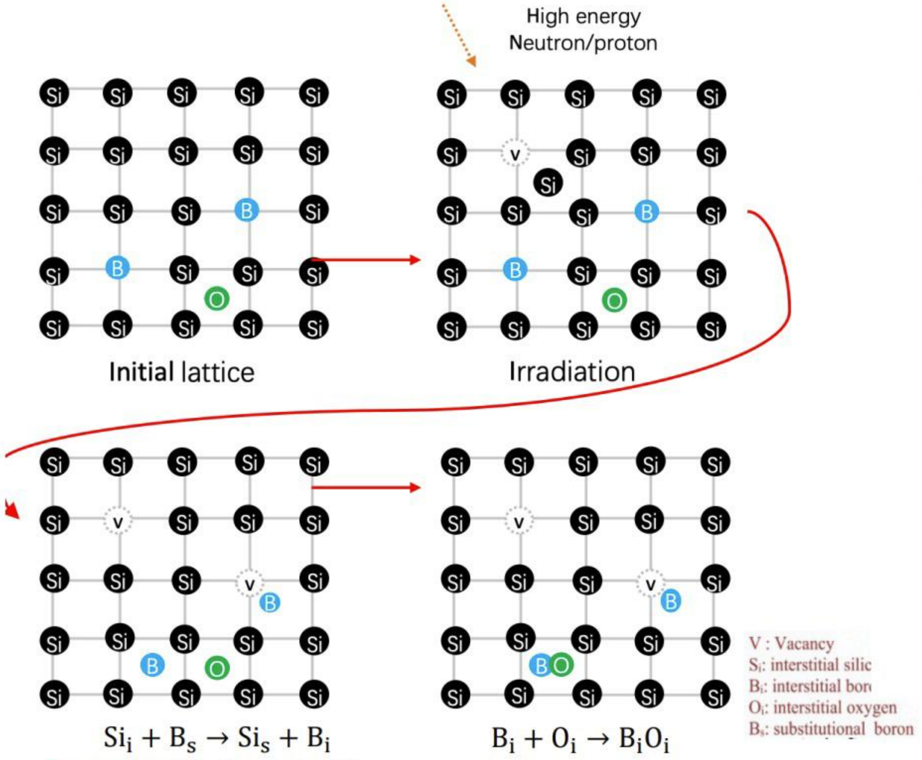
[M.Moll, VERTEX2019]



- Explored use of different gain layer designs, doping materials and C-enriched substrates → **B + C** shows largest gain after irradiation ($C_i + O_i \rightarrow C_iO_i$ competes with $B_i + O_i \rightarrow B_iO_i$)



G.Paternoster, TREDI 2019



Acceptor (B_s) removal in the gain layer after irradiation

The HGTD Modules

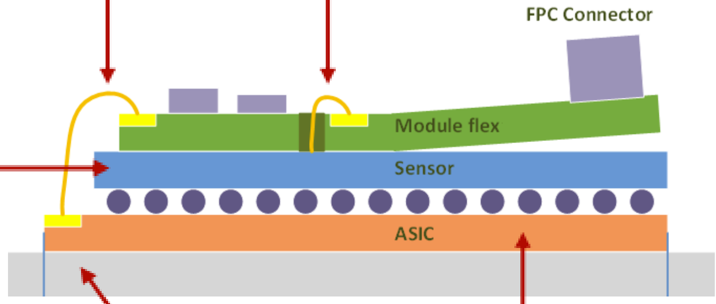
An **HGTD module** consists of:

- Two **sensors** (2 cm × 2 cm)
- Two **ALTIROC ASICs** (2 cm × 2 cm)
- A **module flex**
- A **flex tail**

Wire bonds

HV wire to sensor back-side

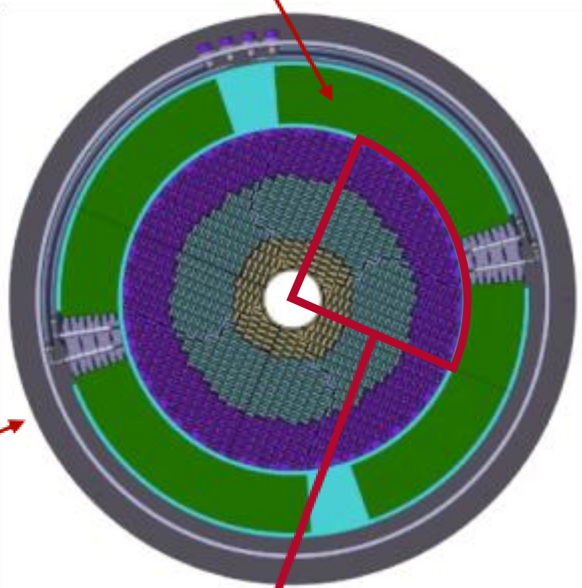
LGAD sensor



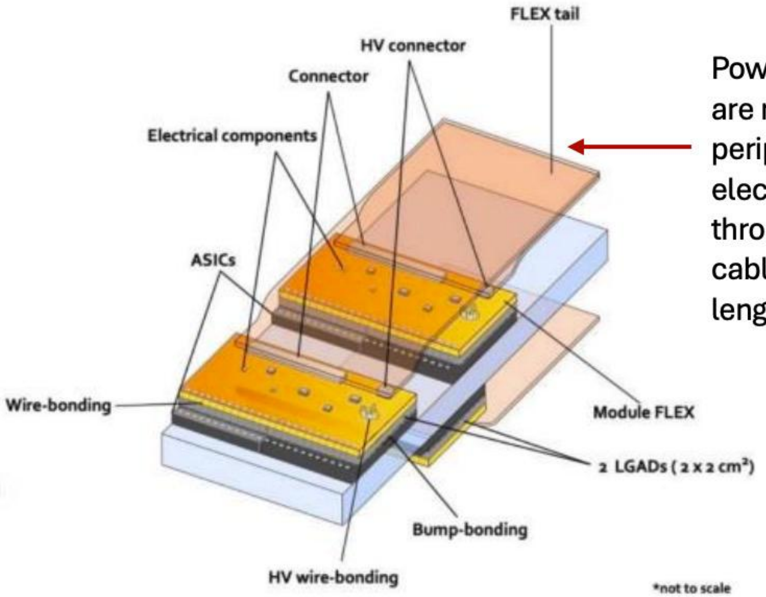
Cooling plate

ASIC bump-bonded to sensor

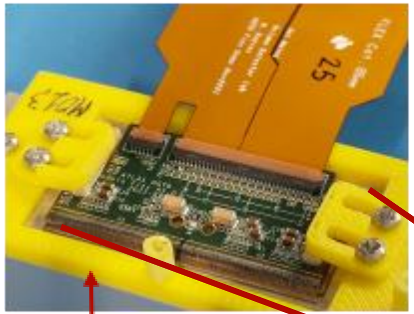
Peripheral Electronics Board (PEB)



An HGTD disk

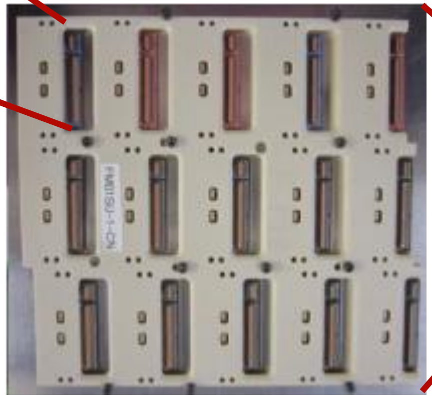


Power and signal are routed to the peripheral electronics through flexible cables of different lengths (flex tail)



Module

Detector Unit (DU)



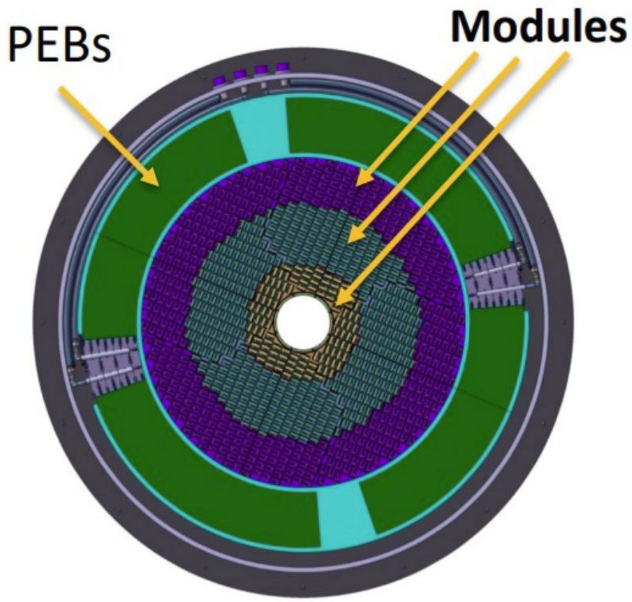
Disk quadrant of the HGTD active region (24DUs)

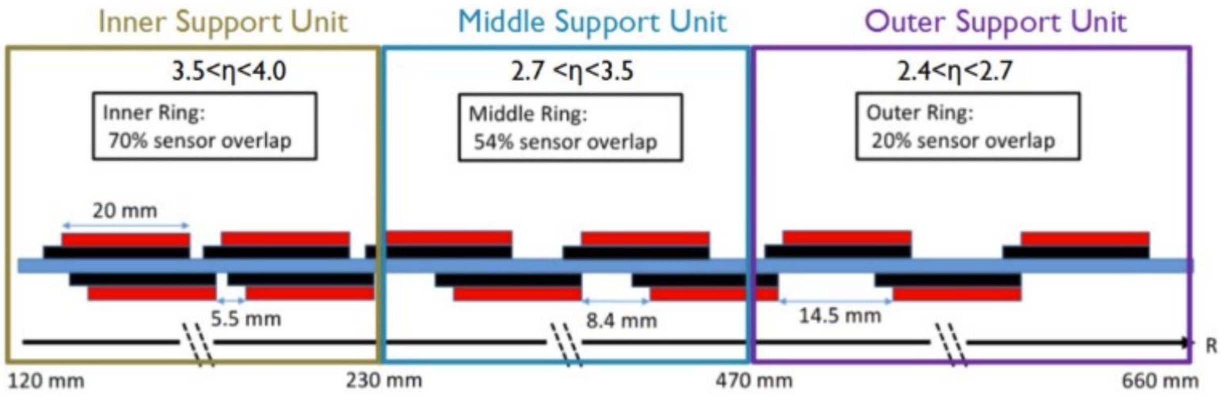
https://indico.cern.ch/event/1469148/contributions/6460347/

HGTD radiation hardness

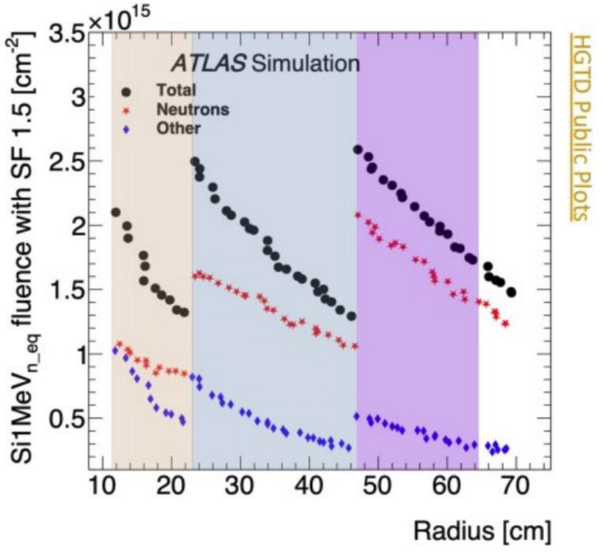
https://indico.cern.ch/event/1307446/contributions/6047182/

- Detector segmented into three independently replaceable rings:





Replaced every 1000 fb^{-1} | Replaced every 2000 fb^{-1} | Can stand the 4000 fb^{-1}

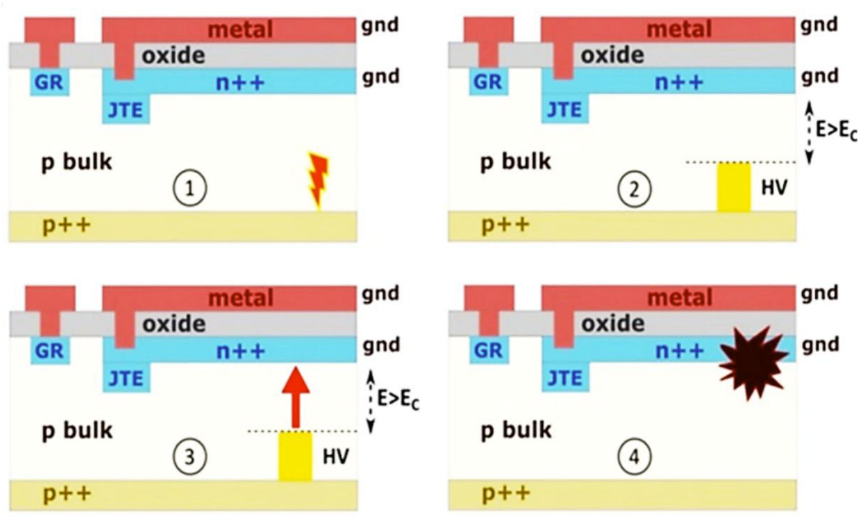


Maximum fluence **2.5 x10^{15} n_{eq}/cm²** and **2 MGy** at the end of HL-LHC (after 4000 fb^{-1})

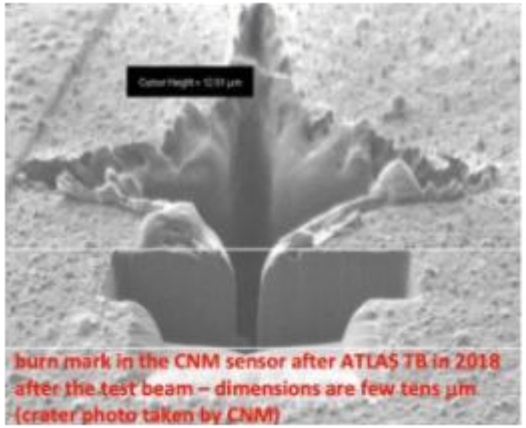
Single Event Burnout (SEB)

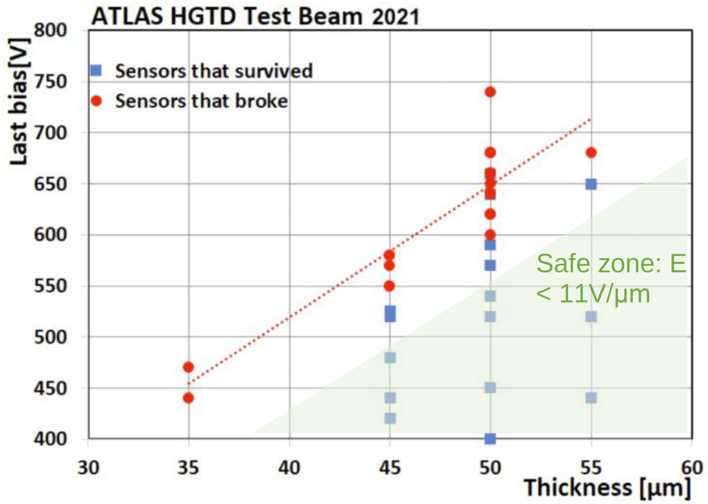
- **Irreversible breakdown** triggered by a large charge deposition at high operation voltages
- Triggered by a **single particle**
- Large energy deposits: **electric field collapse in presence of high concentration of free carriers**
- Observed in several test beam campaigns
- Common effort of **ATLAS/CMS/RD50** collaborations: determine a safe operating voltage
- Systematically studied at HGTD test beams
- Safe operating zone: **11V/µm**

→ For 50µm sensor thickness: **550V**



Source: L.A. Beresford et al. JINST 18 P07030





Sr-90 Test HGTD Hybrid Read-Out