TileCoM Firmware Developments for ATLAS Tile Calorimeter Phase-II Upgrades

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Abstract. The High-Luminosity Large Hadron Collider (HL-LHC) necessitates a comprehensive electronics upgrade of the ATLAS Tile Calorimeter (TileCal) to ensure robust operation under increased radiation and data-rate conditions. To address this, the ATLAS TileCal has introduced the Phase-II upgrade, which involves a complete replacement of the existing electronic system. As part of the Phase-II upgrade, the Tile Computer-on-Module (TileCoM) has been developed to enable real-time monitoring and control of the TileCal Preprocessor (TilePPr) sub-modules. TileCoM provides a critical interface between the Detector Control System (DCS) and TilePPr modules, including the Compact Processing Module (CPM), Advanced Telecommunications Computing Architecture (ATCA) carrier, and Trigger Data Acquisition Interface (TDAQi). TileCoM's firmware integrates the IPbus protocol for register access, I²C for low-level sensor control, and Gigabit Ethernet for high-throughput data transfer, together with a custom Open Platform Communications Unified Architecture (OPC UA) server. Initial validation tests at CERN, conducted using the Avnet Ultra96-V2 development board, successfully demonstrated reliable TileCoM-CPM communication and firmware functionality, marking a key milestone toward current developments.

1 Introduction

The Large Hadron Collider (LHC) is the biggest particle accelerator ever built. It is located at the European Organization for Nuclear Research (CERN) along the Swiss-France boarder [1]. CERN is currently upgrading the LHC into a more powerful version called the High-Luminosity Large Hadron Collider (HL-LHC). The HL-LHC is poised to revolutionize high-energy physics by enabling luminosity levels 5-7 times greater than those of the current LHC [2].

ATLAS is one of the two general-purpose detectors at the LHC at CERN, designed to explore fundamental questions about the nature of matter and the universe. It plays a pivotal role in advancing particle physics, with its most notable contribution being the discovery of the Higgs boson in 2012 [3]. The ATLAS detector uses a hadronic calorimeter to capture and process energy coming from particle collisions from within the LHC. The calorimeter is called the Tile Calorimeter (TileCal) [4].

With the forthcoming HL-LHC upgrades expected to increase the collider's luminosity, the TileCal must undergo significant improvements to handle elevated levels of radiation and data throughput. These changes necessitate a comprehensive upgrade of its readout electronics, including the introduction of the TileCal Preprocessor (TilePPr) boards [5].

2 ATLAS Tile Calorimeter Phase-II Upgrades

The ATLAS TileCal is a hadronic calorimeter system within the ATLAS experiment at the LHC. It plays a vital role in measuring the energy of hadrons, jets and contributes significantly to the identification of missing transverse energy in collision events [6]. As the LHC transitions into the HL-LHC, the need for a major upgrade to the TileCal electronics readout system has become essential.

Figure 1 illustrates the existing electronic readout architecture employed during the standard LHC operations. In this system, signals from the photomultiplier tubes (PMTs) are digitized by the front-end electronics and then passed through a pipeline to the Read-Out Driver (ROD) modules via optical links. While this architecture has been robust, its limitations become apparent under the extreme data rates and radiation environments anticipated in the HL-LHC.

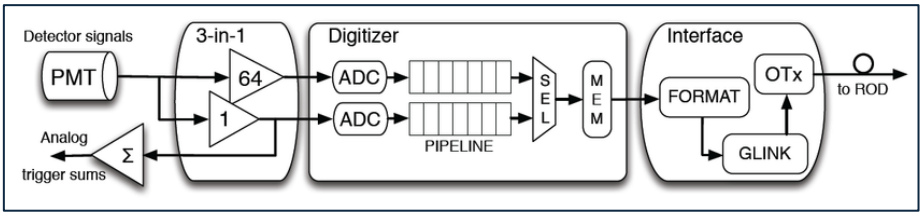

Figure 1: TileCal Electronic Readout Chain for the LHC [7]

To meet the demands of the HL-LHC, a significant redesign of the entire readout chain is being implemented. Figure 2 presents the ATLAS TileCal Phase 2 Upgrade, which introduces a modular and highly parallelized structure.

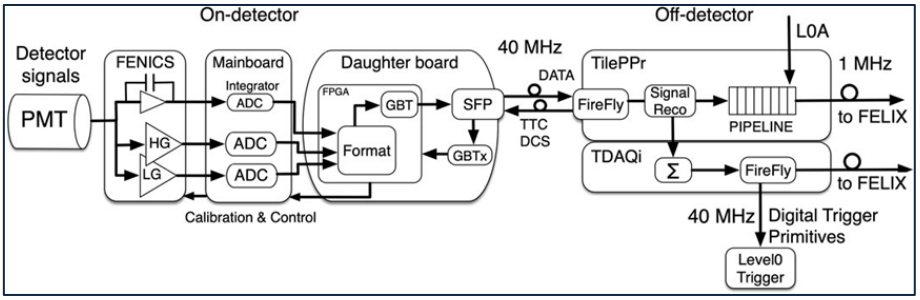

Figure 2: TileCal Electronic Readout Chain for the HL-LHC [8]

The existing LHC TileCal readout system includes 32 ROD boards housed in VME crates, supporting 256 uplinks. The Phase-II HL-LHC upgrade transforms this infrastructure, introducing 32 TilePPr boards housed in Advanced Telecommunications Computing Architecture (ATCA) crates, supporting 4096 uplinks with a total Data Acquisition (DAQ) bandwidth of 40 Gbps. Each TilePPr includes multiple PCBs with FPGAs, Firefly optical transceivers, and power management ICs.

Table 1: Evolving Demands on the Electronic Readout Chain — LHC Compared to HL-LHC [9]

Feature	TileCal (LHC)	TileCal (Phase II Upgrade)
Number of Uplinks	256	4096 (with redundancy)
Uplink Bandwidth	800 Mbps	9.6 Gbps
Number of Downlinks	256	2048
Off-Detector Boards	32 ROD	32 TilePPr
Off-Detector Crates	4 VME	4 ATCA
Bandwidth to DAQ	3.2 Gbps (ROS)	40 Gbps (FELIX)

3 The Tile-Preprocessor

The TilePPr is a critical component of the upgraded TileCal readout system for the ATLAS detector at the HL-LHC. It forms the off-detector electronics of the TileCal for Phase 2 upgrades. The TilePPr processes data signals coming from physical measurements captured by PMTs and interfaces with the Trigger Data Acquisition Interface (TDAQi) to aggregate acceptable events before transferring them to the Front-End LInk eXchange (FELIX) system [10].

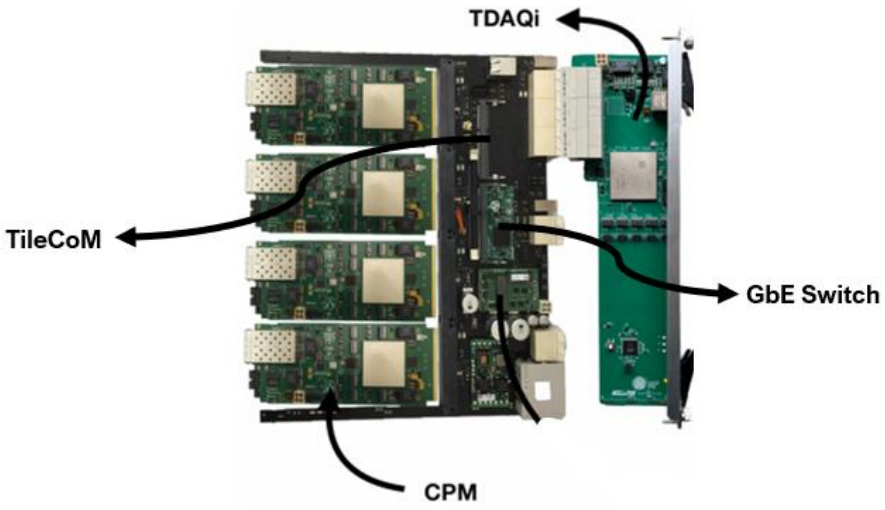

Figure 3: Tile Calorimeter Pre-Processor Module

Figure 3 illustrates the integration of the TilePPr PCBs, developed as part of the ATLAS TileCal Phase-II upgrade. Digitized signals coming from the on-detector electronics are transmitted to the Compact Processing Modules (CPM). Each CPM hosts a Kintex UltraScale Plus (KU+) FPGA. These FPGAs are responsible for the initial stages of data acquisition, formatting, and processing. The input is received via high-speed Firefly optical transceivers. At the centre of the architecture is the Tile Computer on Module (TileCoM), a Zynq-based Multi-processor System on Chip (MPSoC) that serves as the core monitoring and configuration unit. TileCoM interfaces with the ATCA infrastructure, CPMs, and TDAQi through an onboard Gigabit Ethernet (GbE) switch [11]. It also has access to distributed sensors across the system, allowing it to monitor operational parameters such as temperatures, voltages, and currents. The TDAQi board acts as a bridge between the TilePPr and the ATLAS Data Acquisition system. It receives pre-processed data from the CPMs via the ATCA backplane and transmits it to the FELIX using high-speed optical links. It also generates trigger primitives that allow the processing of only useful events from the ATLAS detector

4 Tile-Preprocessor Monitoring Framework

4.1 Software

The software framework supporting TilePPr monitoring is built on the AlmaLinux operating system, running on the Zynq UltraScale+ MPSoC-based TileCoM module. Currently, the TileCoM evaluation board operates using CentOS however, there is an ongoing migration to AlmaLinux.

A key component of the software system is the Open Platform Communications Unified Architecture (OPC UA) server. This server is hosted directly on TileCoM and is responsible for exposing sensor data to the DCS. It is implemented using the Quasar C++ framework, which greatly simplifies OPC UA development by allowing server structures to be defined through XML schema files. Quasar also provides templates and utility modules that make it easier to embed custom data acquisition logic into the OPC UA node tree.

For the testing implementation conducted at CERN, the OPC UA server streamed data to an InfluxDB time-series database through a Telegraf data collector as shown in Figure 4. This intermediate step provided seamless routing of sensor data into a visual analysis environment. Grafana was used as the dashboarding tool to create interactive and real-time plots for various sensor categories.

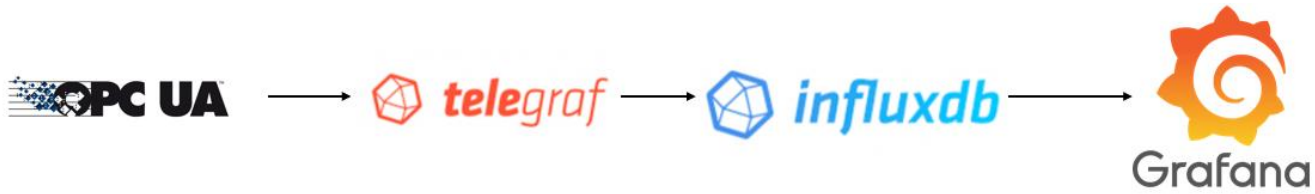

Figure 4: OPC UA Server Integration with Grafana

4.2 Hardware

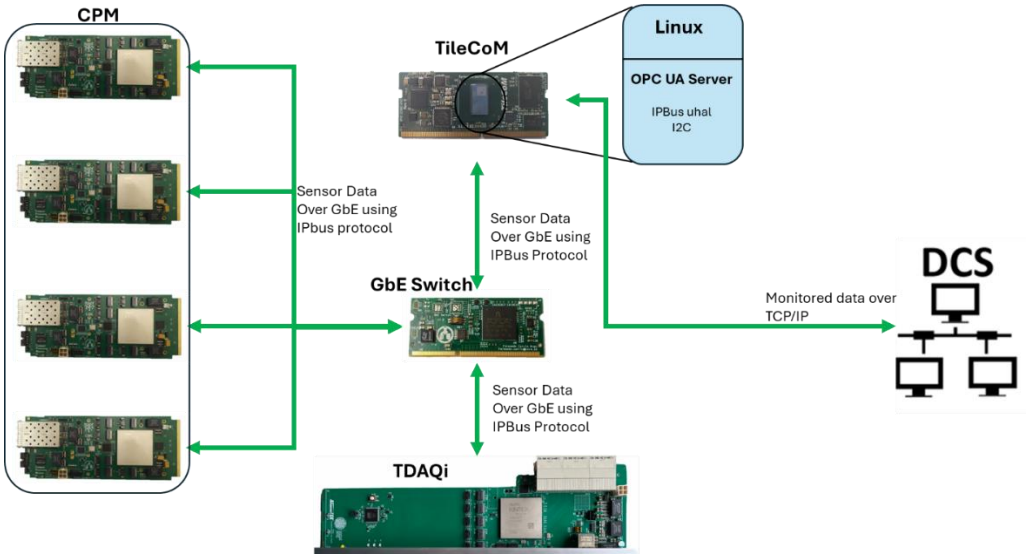

Figure 5: Tile-PPr Monitoring Framework

The hardware monitoring framework of the TilePPr is designed to support high-throughput sensor data acquisition in the demanding environment of the HL-LHC. Each TilePPr unit houses over 1,000 analog and digital sensors distributed across its sub-modules, including the CPM, ATCA board, and the TDAQi. Figure 5 shows how the different TilePPr PCBs are connected together for monitoring through TileCoM

Sensor data acquisition from the TilePPr subsystems is handled through IPbus, a low-level protocol designed at CERN for FPGA register access. IPbus enables TileCoM to poll voltages, currents, and temperatures from distributed TilePPr PCBs such as the CPMs. All sensor data is routed through a Gigabit Ethernet (GbE) switch integrated within the ATCA crate. This switch interconnects the TilePPr PCBs with TileCoM, which serves as the centralized processing node.

Aside from monitoring the off-detector electronics, TileCoM is also used for remotely configuring and programming the FPGAs on the TilePPr PCBs. It also routes provides clocking signals to some of the TilePPr Modules [12]

5 Results From Testing at CERN

To validate the functionality and performance of the developed monitoring system, experimental tests were conducted at CERN using the TileCoM evaluation board interfaced with a CPM. The primary objective was to verify end-to-end data acquisition from onboard sensors using the OPC UA server deployed on TileCoM, with real-time sensor data relayed over GbE via the IPbus protocol. The TileCoM firmware was first installed on the Avnet Ultra96-V2 development board. This board served as a functional prototype for evaluating TileCoM's monitoring capabilities. It was connected to a live CPM unit from the TilePPr assembly.

Figure 6 shows the monitoring data acquired from the CPM through TileCoM. This data was visualized using Grafana. A total of 45 sensor points were actively monitored:

- 10 sensors originated from the TileCoM board itself (MPSoC core voltages and onboard temperature sensors),
- 35 sensors were accessed from the CPM unit, primarily power rails and temperature sensors.

Figure 6: CPM Sensor Data Monitoring and Display over Grafana

5.2 Sensor Data Quality Validation

Following successful data acquisition, a quality analysis was conducted to compare sensor readings against known datasheet specifications. The focus was placed on the CPM's Power Management Unit, which incorporates LTM4644 DC-DC converters. According to the manufacturer's datasheet, these regulators guarantee a voltage regulation accuracy within ±1.5% under nominal conditions. A color-coded validity heatmap (Figure 7) was generated to visualize the percentage of readings that remained within the tolerance band for each sensor over time. Green indicates full compliance (valid data), while red highlights out-of-range or invalid readings. The majority of sensors showed consistent behaviour and remained within the tolerance limits as shown in Figure 7. The temperature IC readings were flagged faulty this is due to an addressing error in the I2C library used. This is currently being corrected.

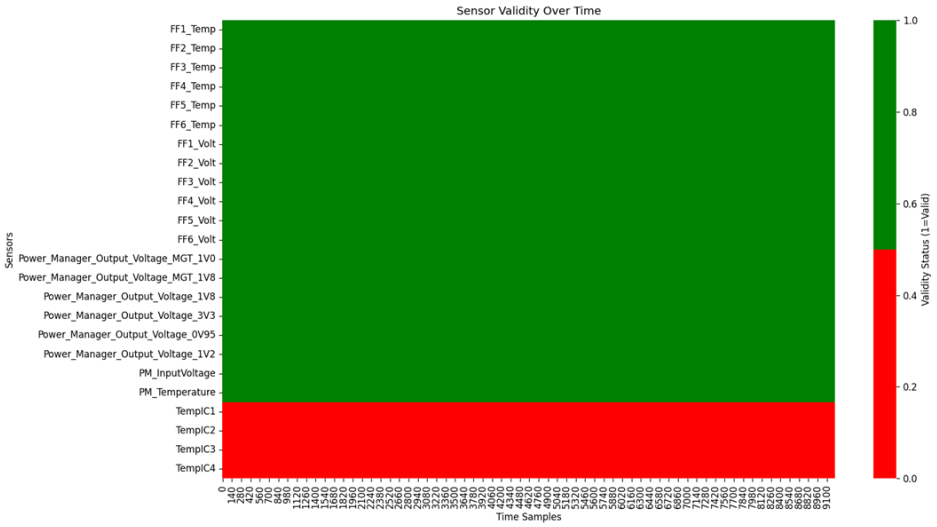

Figure 7: Sensor Data Quality Check on the CPM Power Manager with a ±**1**,**5**% Tolerance

6 Conclusion

This research work addresses a critical challenge in ensuring the functionality and reliability of the upgraded TileCal system within the ATLAS detector at the HL-LHC. The study aims to support the operational demands of the HL-LHC, characterized by higher radiation levels and increased data throughput by designing and implementing a monitoring system for the TilePPr module. The research is expected to provide significant insights into the design and validation of advanced monitoring technologies offering practical benefits to high-energy physics experiments. Additionally, it will establish a framework for future upgrades, ensuring the long-term reliability of the ATLAS detector.

References

[1] L. Evans and P. Bryant, “LHC Machine,” *JINST*, vol. 3, S08001, 2008.

[2] G. Apollinari, O. Brüning, T. Nakamoto, and L. Rossi, “High Luminosity Large Hadron Collider (HL-LHC),” *CERN Yellow Rep.* 2015-005, 2015, arXiv:1705.08830.

[3] G. Aad *et al.* (ATLAS Collaboration), “Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC,” *Phys. Lett. B*, vol. 716, pp. 1–29, 2012.

[4] G. Aad *et al.* (ATLAS Collaboration), “Readiness of the ATLAS Tile Calorimeter for LHC collisions,” *Eur. Phys. J. C*, vol. 70, pp. 1193–1236, 2010.

[5] F. Carrió Argos and A. Valero, “The PreProcessor Module for the ATLAS Tile Calorimeter at the HL-LHC,” *Nucl. Instrum. Meth. A*, vol. 958, p. 162487, 2020.

[6] ATLAS Collaboration, “Operation and performance of the ATLAS Tile Calorimeter in Run 1,” *Eur. Phys. J. C*, vol. 78, no. 12, p. 987, 2018.

[7] F. Carrió and A. Valero, “Clock Distribution and Readout Architecture for the ATLAS Tile Calorimeter at the HL-LHC,” in *Proc. IEEE Real Time Conference*, Williamsburg, VA, USA, Oct. 2018.

[8] ATLAS Collaboration, “Technical Design Report for the Phase-II Upgrade of the ATLAS Tile Calorimeter,” *CERN-LHCC-2017-019*, CERN, 2017.

[9] F. Carrió, P. Moreno, and A. Valero, “Performance of the Tile PreProcessor Demonstrator for the ATLAS Tile Calorimeter Phase II Upgrade,” *JINST*, vol. 11, no. 03, C03047, 2016.

[10] J. Valls et al., "The Readout Architecture of the TileCal Demonstrator Project for the ATLAS Upgrade," IEEE Transactions on Nuclear Science, vol. 67, no. 1, pp. 89–96, Jan. 2020. doi: 10.1109/TNS.2019.2951542

[11],[12] M. G. D. Gololo, Development of TileCoM Firmware and Software for the Off-Detector Electronics of the ATLAS Tile Calorimeter at the HL-LHC, Ph.D. dissertation, Inst. for Collider Particle Physics, Dept. of Physics, Univ. of the Witwatersrand, Johannesburg, South Africa, Aug. 2023.