The South African contribution based on the TileCoM and Tile GbE Switch to the Tile Pre-Processor Modules for the ATLAS Tile Calorimeter: Progress and Current Status.

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Abstract. University of Johannesburg contributes 25% to the final design of the Tile Pre-Processor Modules for the ATLAS Tile Calorimeter at the High-Luminosity Large Hadron Collider (HL-LHC). This work focuses on the status of the Tile Computer-on-Module (TileCoM) and the Tile Gigabit Ethernet Switch (Tile GbE) in terms of firmware, software and hardware integration. The procurement of 62 Xilinx FPGAs for the Control Processing Module (CPM) and 60 Zynq FPGAs for the TileCoM has been initiated, ensuring robust data processing capabilities. Additionally, a dedicated test station at the University of Johannesburg has been established to integrate the TileCoM, Tile GbE, and CPM for validation in terms of sensor data acquisition and performance testing. Significant progress has also been made on the TileCoM's Open Platform Communications Unified Architecture (OPC UA) server, a key component for remote control and monitoring. This presentation provides an update on these developments, highlighting South Africa's vital contributions to the ATLAS Tile Calorimeter Phase-II upgrade.

1 Introduction

The Large Hadron Collider (LHC) at CERN is the world's most powerful particle accelerator, enabling discoveries in fundamental physics. In preparation for its next evolution, the High Luminosity LHC (HL-LHC) aims to increase the instantaneous luminosity by a factor of 5 to 7 beyond the original design of the LHC [1]. With data-taking expected to begin in 2029, the HL-LHC will enhance the physics reach of experiments like ATLAS, providing a tenfold increase in the accumulated dataset.

The ATLAS detector is a general-purpose experiment designed to study Higgs physics, possible physics beyond the Standard Model, and electroweak symmetry breaking. The Tile Calorimeter (TileCal), a sampling hadronic calorimeter made of steel absorbers and scintillating plastic tiles, is the central component of ATLAS's calorimetric system. It is separated into two extended barrels and a central barrel. Photomultiplier tubes (PMTs) read out each module that is further divided into barrel sections [2].

A front-end system installed on the detector and a back-end system situated in the counting room make up the current TileCal readout chain. Analog data is sent to the Digitizer Boards for digitization and data transfer through the Read-Out Drivers (RODs) after the front-end boards amplify and shape PMT signals [3].

This paper presents the South African (SA) contribution from the University of Johannesburg (UJ) to the ATLAS Tile Calorimeter. UJ contributes 24% towards the final design of the off-detector electronics for the ATLAS Tile Calorimeter Phase-II upgrades. Figure 1 presents the ATLAS Tile Calorimeter current electronic readout system. This electronic readout system is not able to accommodate the HL-LHC requirements.

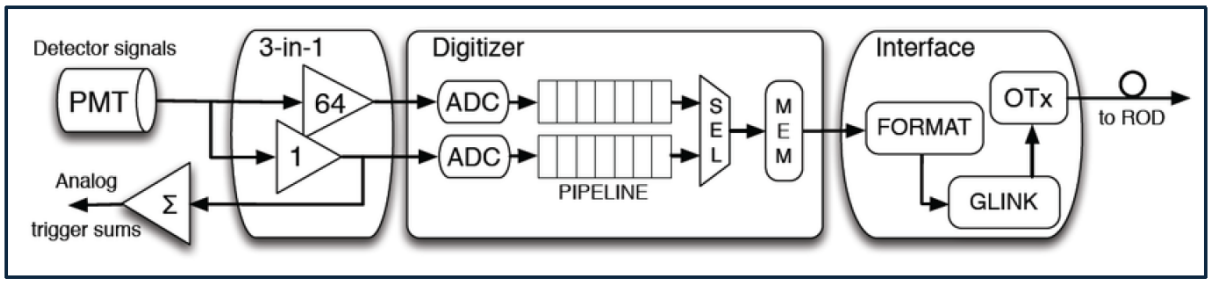

Figure 1: The ATLAS Tile Calorimeter current electronic readout system [3]

2 ATLAS TileCal Phase-II

An important component of the larger ATLAS Phase-II endeavor is the TileCal Phase-II Upgrade. A fully digital and redundant system will replace the entire readout chain as part of the update [4]. Redesigned Front-End Boards (FEBs), Main Boards (MBs), Daughter Boards (DBs), and a potent off-detector module known as the Tile PreProcessor (TilePPr) are all part of the new architecture as presented in Figure 2 [5].

The back-end system's primary component is the TilePPr [6]. It interfaces with the ATLAS Trigger and Data Acquisition (TDAQ) system, processes data in real-time, and receives high-speed optical data from all FEBs. It has a bespoke Ethernet switch, data buffering, timing modules, and Field-Programmable Gate Arrays (FPGAs) [7].

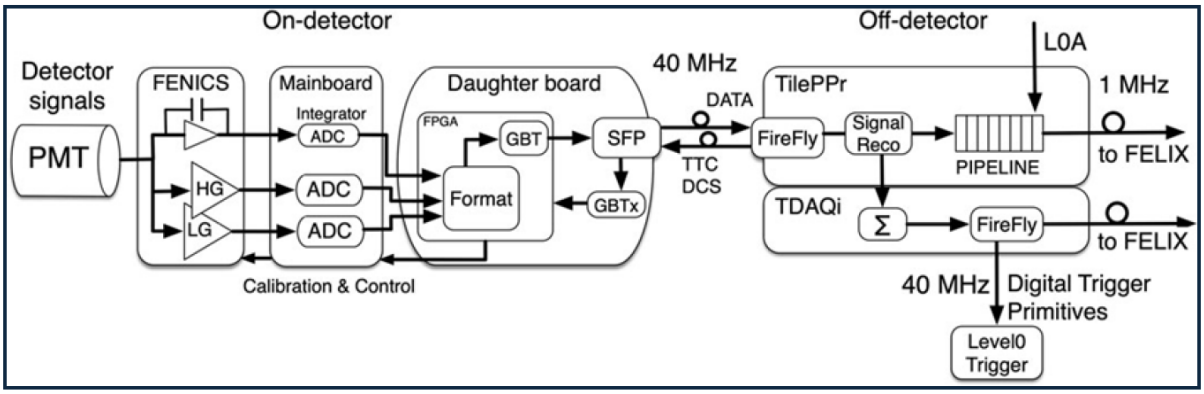

Figure 2: The ATLAS Tile Calorimeter Phase-II upgrade electronic readout system [5]

Redundancy and radiation-hardness were key considerations in the design of the entire system, which allows for smooth functioning even in the severe circumstances anticipated in the HL-LHC period [8].

2.1 Tile Computer On-Module (TileCoM)

For slow control and system monitoring, the TilePPr has a small embedded control module called the Tile Computer On-Module (TileCoM) shown in Figure 3. It functions as a Linux-based Zynq UltraScale FPGA platform that supports several I/O protocols (I2C, SPI, UART, and GPIO) and has Ethernet connectivity. Voltage, temperature, and current sensors are among the TilePPr components whose configuration and health monitoring are controlled by the TileCoM. Additionally, it offers a web interface for firmware management and remote diagnostics. During HL-LHC operation, the TileCoM, which was partially developed by the UJ, is essential for guaranteeing the dependability and real-time diagnostics of the off-detector electronics[9, 10].

2.2 Tile GbE Switch

In order to provide internal data routing between its different TilePPr modules, including communication with the TileCoM, Control Processing Module (CPM), and TDAQi, the Tile GbE Switch (Figure 4) is a specially created Ethernet switching module integrated within the TilePPr. The switch is designed for redundancy and low-latency

Figure 3: The Tile Computer On-Module (TileCoM)

communication, and it supports several Gigabit Ethernet channels. It makes it possible for the TilePPr's control, monitoring, and data streaming features to be seamlessly integrated. The UJ has conducted extensive testing and signal integrity validation, and South African industry partners Trax Interconnect and Jemstech have been in charge of PCB production [11]. Its effective implementation improves the TileCal data collecting system's overall flexibility and maintainability.

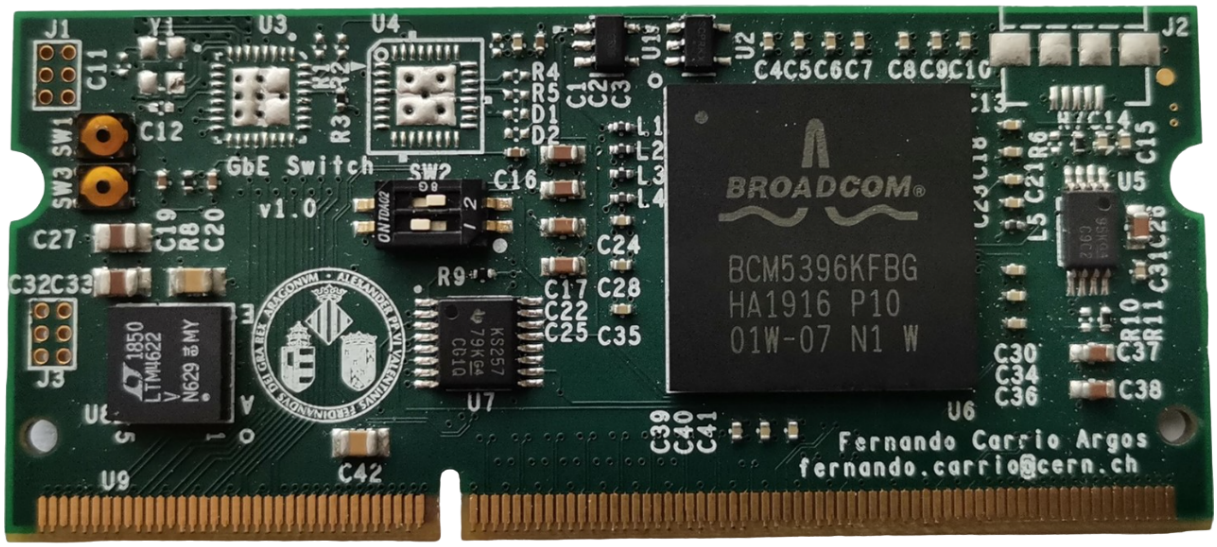

Figure 4: The Tile GbE Switch

3 UJ ATLAS TileCal Phase-II Projects

As mentioned above that UJ is contributing 24% towards the final TilePPr design. This is in terms of both the hardware and firmware developmens. At UJ, three main initiatives have been led:

3.1 Control and Monitoring via TileCoM

The TilePPr is slowly controlled, monitored, and configured by the TileCoM, an embedded system. It delivers Ethernet-based diagnostics, handles firmware updates via network protocols, and reads out sensor data (temperature, voltage, and current). UJ created unique firmware in VHDL and C++ to support SPI, UART, and I2C protocols. Figure 5 shows the control and monitoring results via TileCoM.

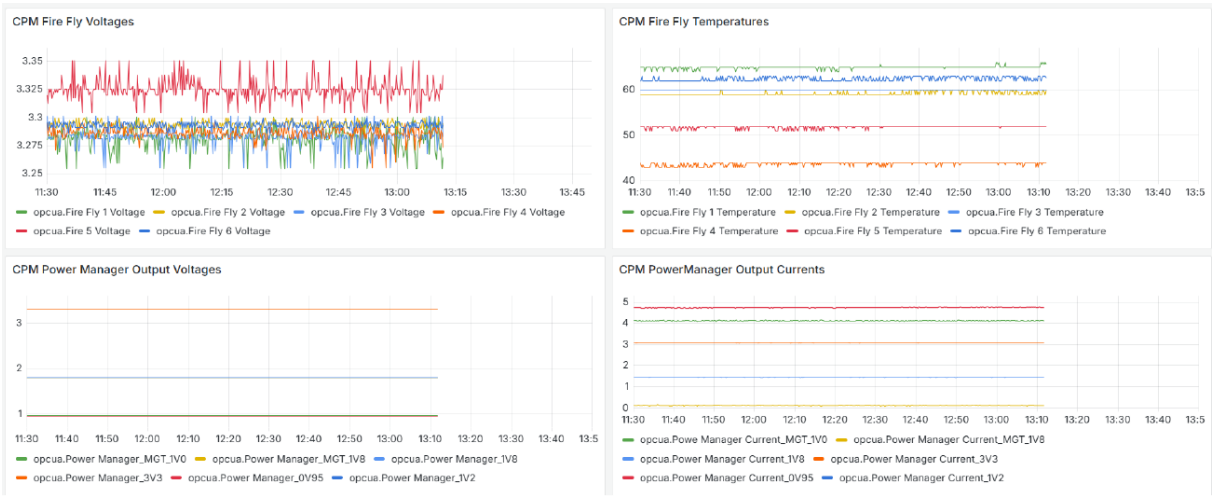

Figure 5: Control and Monitoring results via TileCoM

3.2 Testing of the Tile GbE Switch PCB

Another addition from UJ is the Tile GbE Switch, which makes it easier for internal subsystems to communicate via Ethernet. High-bandwidth oscilloscopes were used to perform signal integrity checks, which included signal trace loss measurements, jitter measurements, etc. The carrier board and TileCoM have been successfully integrated with the switch. Figure 6 shows the results for the differential plot for S22 and S11 parameter on the left and, the difference in error between adapters S22 and S11 shows that there is no error between the two adapters for S22 and S11 on the right.

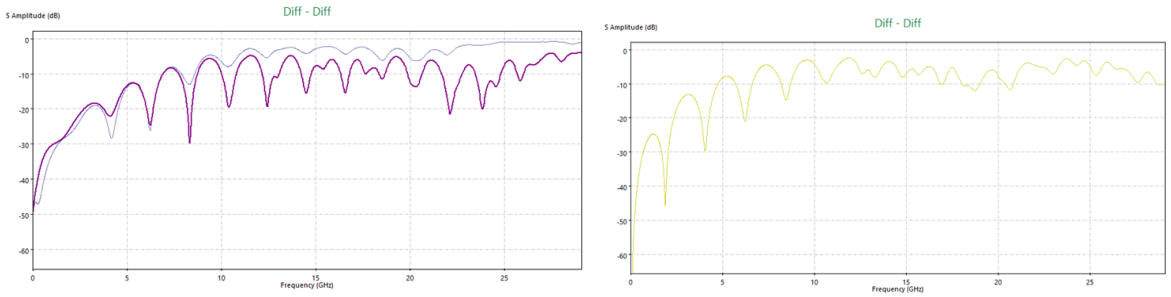

Figure 6: (*left*) The differential plot for S22 and S11 parameter. (*right*) The difference in error between adapters S22 and S11 shows that there is no error between the two adapters for S22 and S11.

3.3 Predictive ML for Anomaly Detection

UJ is using machine learning (ML) technologies to examine sensor data from the TileCoM in order to guarantee long-term operational integrity. Anomalies are predicted beforehand using time-series models. A real-time web dashboard is used to visualize the data in this work, which makes use of the PyTorch and Scikit-learn frameworks [12, 13]. Figure 7 shows the machine learning model flowchart and the results using the predicted and the test data.

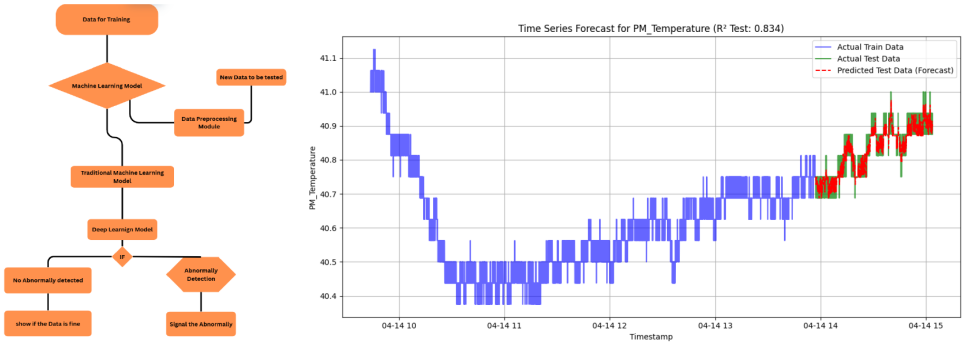

Figure 7: (*left*) The machine learning model flowchart . (*right*) The machine learning model predicted results (red dashed line) are consistent with the test data shown in green.

4 TilePPr Pre-production status and test bench

At UJ, a specific test bench was set up for the purpose of functionally validating each TilePPr subsystem. TileCoM, a GbE switch, FPGA commercial boards, oscilloscopes for validating analog signals and a 12V DC power supply with programmable current limitations are all included in the bench. To verify communication stability, power integrity, and inter-module compatibility, integration tests have been conducted. Pre-production testing is in line with the TileCal Phase-II commissioning schedule as of July 2025.

Figure 8: UJ-TilePPr test bench

Figure 8 shows the UJ-TilePPr test bench used to test the PCBs before they can be shipped to CERN for insertion in the Tile Calorimeter electronic system. There are ongoing minor firmware improvements, especially in TileCoM's monitoring and exception-handling capabilities. In Q4 2025, full pre-production deployment is anticipated.

5 Conclusion

The HL-LHC's unparalleled radiation environment and data volume present urgent requirements that the ATLAS TileCal Phase-II upgrade attempts to meet. The UJ is a prime example of South Africa's increasing dominance in detector electronics, embedded firmware, and machine learning applications for instrumentation thanks to its substantial contributions to the TilePPr system.

The integration of the last pre-production components at CERN and getting ready for the full system commissioning in 2027–2028 will be the main goals of future development. The cooperation between UJ, CERN, and regional businesses serves as a strong example of long-term, international scientific collaborations.

6 Acknowledgement

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