# Ongoing validation of the High Granularity Timing Detector (HGTD) demonstrator for the ATLAS phase II upgrades

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**Abstract.** The High Granularity Timing Detector (HGTD) demonstrator was developed to validate the design and performance of its components. The setup included a printed circuit board (PEB), 58 modules, flex tails, a cooling system, and a data acquisition (DAQ) server. Tasks performed involved connecting flex tails, conducting alignment and Inter-Integrated Circuit (I2C) tests, and performing scanning tests to check bump connections. Threshold voltage (Vth) scans were conducted with high voltage (HV) off at different injected charge values to verify electrical contact between readout electronics and the sensor. Module tuning and charge scans were performed by analysing the time-over-threshold (TOT). A comparison of Vth scans with HV both off and on was done to validate module performance. I2C test failures and high voltage issues, such as large leakage current causing modules to turn off, were identified. Furthermore, clock jitter measurements and calibration methods, mitigating pile-up effects in the forward region, were intended to ensure that the detector's timing capabilities meet specifications and to identify potential issues with clock distribution or signal integrity. In parallel, work progressed on the second-generation demonstrator, incorporating a slice of the prototype vessel with final design features and an increased number of active components to further refine and validate the HGTD design and its integration aspects, such as the Faraday cage.

## 1 Introduction

With the ATLAS experiment undergoing phase II upgrades, a new detector called High Granularity Timing Detector (HGTD) shown in Figure 1 will be installed in the endcaps to cope with the challenge of mitigating pileup effects experienced on the High Luminosity Large Hadron Collider (HL-LHC) [1], which are the product of proton-proton collisions, they create overlapping signals that distort the reconstruction of precise event vertices. With the quick timing capabilities of the HGTD to differentiate tracks coming from closely spaced vertices by utilising their time separation.

The HGTD covers a radial range from 12 cm to 64 cm and geometrically, it occupies a psuedorapidity range of ($2.4 < \eta < 4.0$). Low Gain Avalanche Detectors (LGADs) with small pixel size of $1.3 \times 1.3$ mm$^2$ to reach good time resolution of approximately 30 ps per track. The design makes sure there is high radiation tolerance up to fluences of $3.7 \times 10^{15}$ neq/cm$^2$, doses of 4.1 MGy, depending on the radial distance, an average hit count of 2 to 3 per track and low occupancy below 10%, which is suitable for the harsh environment of the HL-LHC [3].

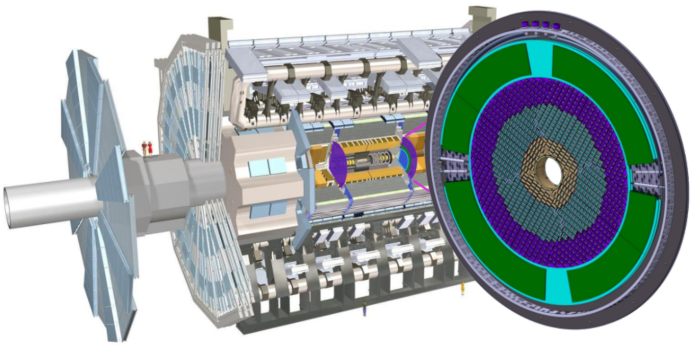

Figure 1: Schematic of the major upgrades to the ATLAS detector for the HL-LHC era, with HGTD location shown [2].

### *1.1 Physics motivation*

There is more role played by the HGTD which extends beyond pileup suppression. It significantly enhances the identification of Higgs boson signal and improves measurements sensitive to the weak mixing angle, particularly in forward and cental-forward electron channels. With the timing information precise luminosity measurements with a linear relation linking pileup density and the number of HGTD hits shown in Figure 2, which are important for accurate Higgs boson studies.

*1.1.1 Pile-up Challenge at HL-LHC* At the HL-LHC, pileup from simultaneous proton-proton interactions causes a huge challenge for event reconstrution and particle identification. Regardless of the collisions occurring in close proximity, there is a separation in time leading to noisy conditions. The HGTD aims to use precise timing to classify signals belonging to the primary collision vertex from pile-up background, thereby completely limiting pile-up contamination.

*1.1.2 Impact of HGTD* The HGTD's timing information, with resolution of $\sim$30 ps, allows:

- Separating electrons from pile-up jets associated with timing differences, forward electron identification is enhanced [3].
- In forward regions with high pile-up, there's an improved precision in measurements of the weak mixing angle, a important electroweak parameter [3].
- Sensitivity gains in Drell–Yan processes of approximately 13% in Central–Forward and 25% in Forward–Forward lepton pair production channels [3].
- Increased electron purity enables higher precision electroweak physics.

*1.1.3 Luminosity Measurement* For Higgs boson physics, a precision luminosity measurements ($\sim$1%) is important. The HL-LHC campaign demands HGTD's high granularity results in low occupancy and linear hit rate response, facilitating bunch-by-bunch luminosity estimation using fast readout [3].

## 2 Overview of the HGTD Demonstrator

The HGTD demonstrator serves as a testbed to validate the design, performance, and integration of HGTD components before final installation. The demonstrator aims to evaluate key parameters such as sensor timing resolution ($\sim$30 ps), radiation hardness, thermal performance, and mechanical and electrical integration.

*Demonstrator components and setup*:

1. LGAD sensor modules: 54 modules assembled with readout Application Specific Integrated Circuit (ASIC)s.
2. Power Supply: High Voltage (HV) applied to fully deplete sensors; Low Voltage (LV) powers front-end electronics.

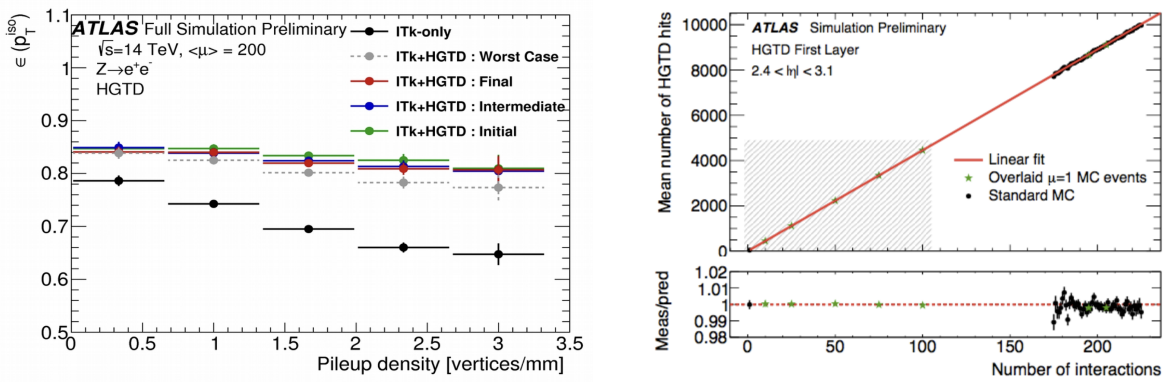


Figure 2: (*left*) Electron isolation efficiency as a function of pileup density ($\mu$). Without timing, the Inner Trackers (ITk)'s efficiency deteriorate significantly at high $\mu$. Whereas the ITk and HGTD system maintains performance, especially with sharper timing resolution. The increasing distance between curves points out the HGTD's important role in suppressing pileup-induced fake hits. (*right*) Linearity between number of hits as a function of average number of interactions per bunch crossing (pileup) [4] .

3. Peripheral Electronic Board (PEB): Distributes power, monitors environmental conditions (temperature and humidity), and interfaces with the data acquisition (DAQ) system [5].
4. Flex tails: For signal and power routing to and from the detector modules.
5. $CO_2$ cooling system: Maintains thermal stability under realistic power loads.
6. DAQ server: Controls synchronised data acquisition [6].

These components form the integrated test setup representing key aspects of the final HGTD system design.

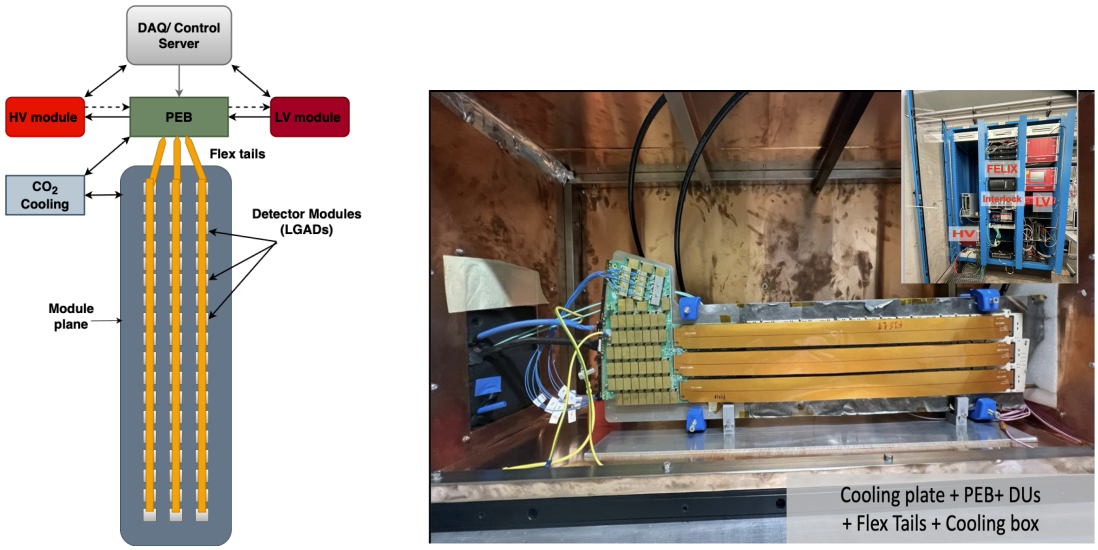


Figure 3: (*left*) Schematic of the HGTD demonstrator. (*right*) The actual demonstrator and its components located at CERN.

## 3 Validation and Test Results

### *3.1 Initial tests and alignment*

- Alignment tests: Required all IpGBT (Low-Power Gigabit Transceiver) links to be correctly aligned before data taking [7]. Alignment involves disabling equalisation and enabling pre-emphasis on the transceivers

using a preparatory python script. Most channels aligned successfully; a few required power cycles and re-initialisation.

- Inter-Integrated Circuit (I2C) communication: The I2C test phase verified communication between PEB and the modules by writing and reading back register values. Some modules failed these tests, indicating issues with components or module integration .

- Bump Bonding checks: Threshold scans were performed with sensor bias both ON and OFF to verify bump bonding and charge collection efficiency. Threshold scans involved injecting known calibration charges and scanning the discriminator threshold of the front-end electronics. Threshold scans are a important diagnostic and quality assurance tool used during the assembly and validation of the HGTD modules. These scans help verify electrical connectivity, bump-bond integrity, and sensor performance at an early stage and before deployment. Sigmoid (S)-curves are a diagnostic tool to used ensure all pixels respond uniformly to injected charges, identify faulty bump bonds or sensor defects and calibrate thresholds for optimal detector performance.

### *3.2 Threshold scan analysis*

With HV off, electronic response was measured for charges of 12 and 36 DAQU units to establish baseline noise and threshold behaviour. This was done to verify good electrical connectivity between the HGTD module's readout electronics and the LGAD sensor. With HV applied, full sensor depletion enabled improved charge collection, as evident from shifts in discriminator thresholds. The difference between on and off scans highlighted disconnected or weak bumps that degrade detector efficiency as shown in Figure 4. The charge collection efficiency when HV is OFF diffuses slowly with lower signal-to-noise, this is seen with broader S-curves and when HV is ON, charge collection is accelerated by electric field, S-curves have a sharper transition, confirming good operation.

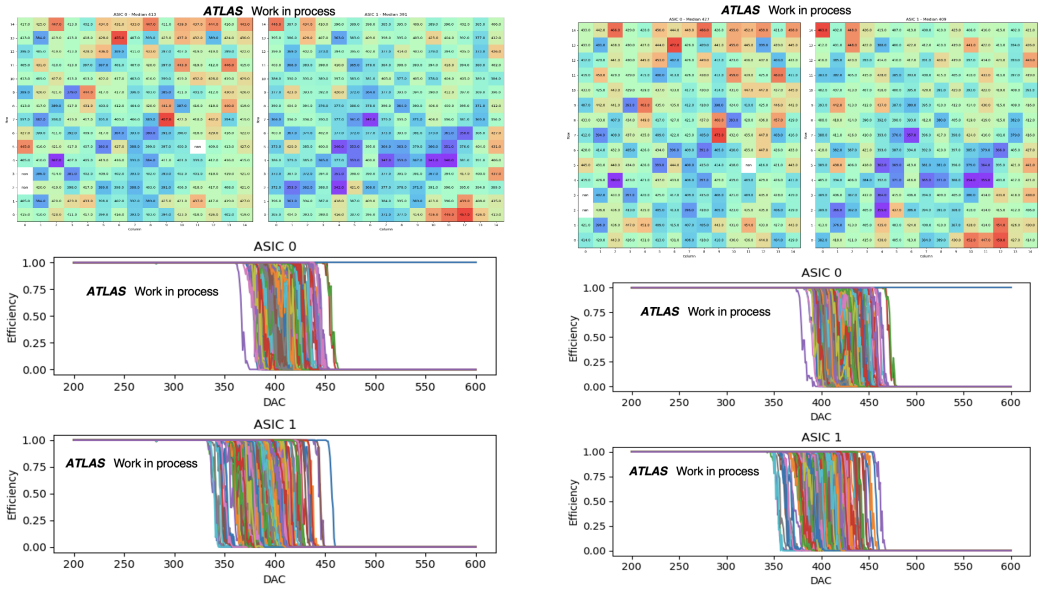


Figure 4: (*left*) Threshold scan with HV OFF with charges set, S-curves are broader due to diffusion-dominated charge collection. (*right*) Threshold scan with HV ON, S-curves become steeper, confirming charge collection through the electric field.

The resulting 2D maps shown in Figure 5 represent the perpixel response across the ASIC matrix. Each pixel encrypts the response through a color scale: green for functioning channels (HV OFF), red for disconnected or non-functional pixels, and a quantitative gradient (HV ON) indicating threshold DAC values or signal amplitude. The maps allows identification of dead pixels appearing as red (HV OFF) or as saturated outliers in HV ON scans, typically indicating complete bump disconnection. Weak or degraded connections are viewed with intermediate or inconsistent colours, and are correlated with partial signal loss or increased noise. Whereas hot pixels with elevated thresholds or excessive response under HV, potentially indicative of leakage or radiation-induced effects. The difference between HV ON and HV OFF scans shown in the bottom plots, confirms the presence of both

stable and unstable regions across the ASIC. While the majority of pixels exhibit minimal variation, isolated clusters show significant shifts, hinting at systematic bonding issues or localised stress which can either be thermal or mechanical. Pixels near ASIC edges tend to be more susceptible, possibly due to layout constraints or tooling imprecision during bonding. Modules with >5% of disconnected or noisy pixels are flagged for further inspection or rework, as such defects directly impact charge collection efficiency and, consequently, the HGTD's timing resolution. This correlation is further supported by the absence or distortion of S-curve behaviour in threshold scans for affected pixels.

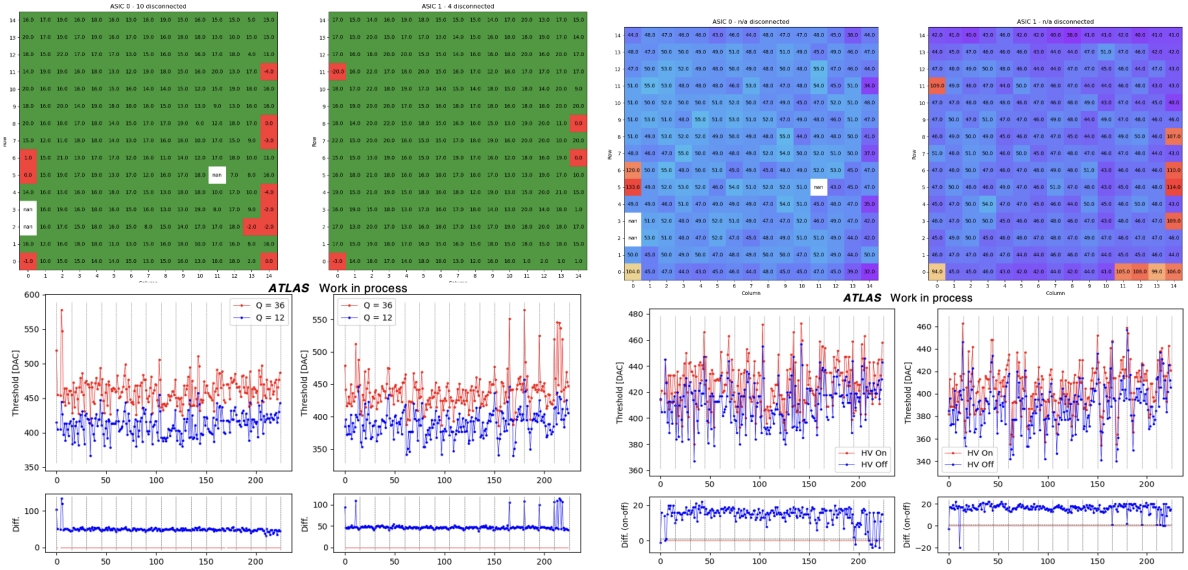


Figure 5: (*left*) Top: 2D threshold maps for two ASICs, comparing HV OFF and HV ON (*right*) setups. Green pixels is when HV OFF which indicates functional bump bonds, while red pixel indicates disconnected channels. HV ON maps (colour gradient) reveal elevated thresholds (orange/red) in noisy or unstable pixels under bias. Bottom: Threshold distributions and difference plots demonstrate stable behaviour for most pixels, with localised spikes highlighting bump bond defects or HV induced instabilities particularly near ASIC edges.

### *3.3 Power and Thermal Tests*

An extensive power tests were conducted to validate the electrical performance and stability of the HGTD demonstrator. Both HV and LV systems were successfully integrated into the Detector Control System (DCS), enabling remote operation, current monitoring, and over current protection with a set point at 200 $\mu$A per module. All 54 modules were powered and monitored to evaluate current draw and tripping behaviour. Under full load, system temperature increased from $\sim$20 °C to 42 °C, confirming the effectiveness of the $CO_2$ cooling system. LV channels drew expected currents based on demonstrator parameters (11.4 V, 0.16 Ω), with 10.6 A and 12.7 A measured using two channels with 25 and 29 modules, respectively. The tests are important in validating the electrical readiness and ensuring safe, scalable operation under realistic HL-LHC conditions.

## 4 Test beam activities

A preliminary test beam study was conducted to evaluate the performance of the HGTD demonstrator using the full readout chain. Three modules were connected through long flex tails to the PEB and operated at 1280 Mbps positions, interfacing with FELIX readout. Alignment and lpGBT configuration were successful; however, communication with the ALTIROC readout chip proved unstable, leading to frequent errors. These tests highlighted key integration challenges in the full DAQ chain and emphasised the need for further debugging and optimisation of the control firmware and interface configuration for future beam campaigns.

## 5 Summary and outlook

The HGTD demonstrator has reached a significant milestone with the successful integration of HV, LV, and interlock systems into the DCS framework. All functional modules can now be remotely operated and monitored

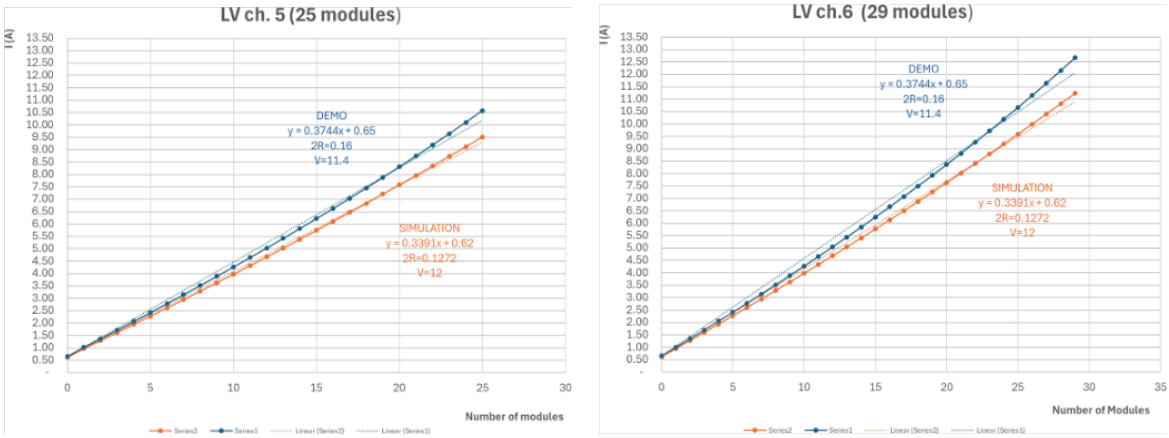


Figure 6: Comparison between simulated and demonstrator power parameters on different channels. The simulation assumes 12 V and 0.1272 Ω, while the demonstrator operates at 11.4 V and 0.16 Ω.

through the DAQ software, which has been recently introduced to automate and simplified the testing process. In parallel, a second-generation demonstrator is under development, incorporating a Faraday cage for improved electromagnetic shielding. These developments ensure that the demonstrator is well-positioned for continued validation, including upcoming beam tests and environmental qualification studies in preparation for deployment in the ATLAS Phase-II upgrade.

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